SCM3000C Series

Data Sheet

Description

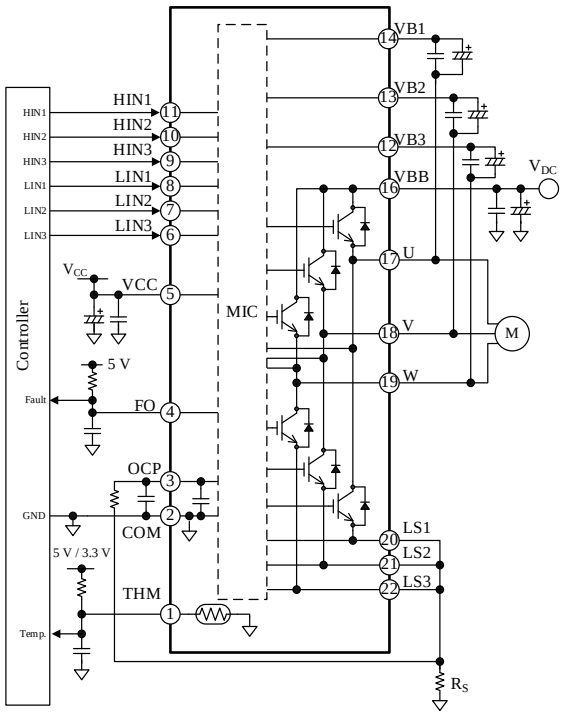
The SCM3000C series are 3-phase brushless motor driver ICs in which output transistors, a pre-driver IC (MIC), bootstrap diodes with current-limiting resistors, and a temperature-sensing thermistor are highly integrated.

These products can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

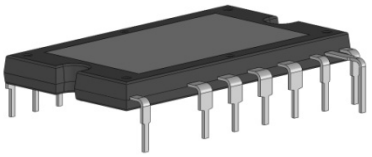
- Built-in Thermistor
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Dead Time: 0.9 µs (min.)
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Isolaton Voltage: 2000 V (for 1 min)
- In Case of Malfunction, All Outputs Shut Down at Once
- Fault Signal Output at Protection Activation
- Protections:
  Undervoltage Lockout for Power Supply
  High-side (UVLO_VB): Auto-restart
  Low-side (UVLO_VCC): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Simultaneous On-state Prevention: Auto-restart

Typical Application

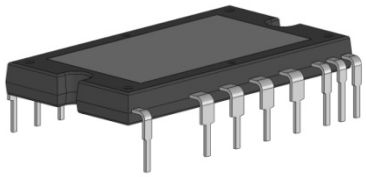


Packages

DIP22
Pin Pitch:
2 mm at Low Pin-to-Pin Voltage Difference
4 mm at High Pin-to-Pin Voltage Difference
Mold Dimensions: 38 mm × 20.8 mm × 4 mm



Leadform 2581



Leadform 2582

Not to scale

Selection Guide

- IGBT + FRD (600 V)

I_O (A)	Part Number	Feature
10 A	SCM3610C11	Low noise
15 A	SCM3615C11	Low noise

Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Air Conditioner Compressor Motor
- Washing Machine Main Motor
- Fan Motor
- Pump Motor

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB–LSx	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LSx	500	V	
IGBT Breakdown Voltage	V_{CES}	V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600	V	
Logc Supply Voltage	V_{CC}	VCC–COM	20	V	
	V_{BS}	VB1–U, VB2–V, VB3–W	20		
Output Current(1)	I_O	T_C = 25 °C, T_j < 150 °C	10	A	SCM3610C11
			15		SCM3615C11
Output Current (Pulse)	I_{OP}	T_C = 25 °C, $P_W \leq$ 1 ms, single pulse	20	A	SCM3610C11
			30		SCM3615C11
Input Voltage	V_{IN}	HINx–COM, LINx–COM	−0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO–COM	−0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCP–COM	−5 to 7	V	
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 125	°C	
Junction Temperature(3)	T_j		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	
Isolation Voltage(4)	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2000	V	

(1) Should be derated depending on an actual case temperature. See also Section 15.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the monolithic IC (MIC), transistors, and freewheeling diodes.
(4) Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–COM	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCC–COM	13.5	—	16.5	V	
	V_{BS}	VB1–U, VB2–V, VB3–W	13.5	—	16.5	V	
Input Voltage (HINx, LINx)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs	
	$t_{IN(MIN)OFF}$		0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		0.9	—	—	µs	
FO Pin Pull-up Resistor	R_{FO}		1	—	22	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF	
Thermistor Noise Filter Capacitor	C_{THM}		4.7	—	—	nF	
Thermistor Pull-up Resistor	R_{THM}		4.4	—	—	kΩ	
Bootstrap Capacitor	C_{BOOT}		10	—	220	µF	
Shunt Resistor	R_S	$I_P \leq 20$ A	27	—	—	mΩ	SCM3610C11
		$I_P \leq 30$ A	18	—	—		SCM3615C11
PWM Carrier Frequency	f_c		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V.

3.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC–COM	9.5	10.5	11.5	V	
	$V_{BS(ON)}$	VB1–U, VB2–V, VB3–W	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC–COM	9	10	11	V	
	$V_{BS(OFF)}$	VB1–U, VB2–V, VB3–W	9	10	11	V	
Logic Supply Current	I_{CC}		—	1.8	—	mA	
	I_{BS}	VB1–U, VB2–V, VB3–W = 15 V; HIN = 5 V; VBx pin current per phase	—	140	—	µA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx)	V_{IH}		1.5	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx)	V_{IL}		1.0	1.5	2.0	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	µA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	µA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	—	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
Overcurrent Protection Threshold Voltage	V_{TRIP}		0.475	0.500	0.525	V	
Overcurrent Protection Hold Time	t_P		20	30	—	µs	
Overcurrent Protection Blanking Time	t_{BK}	V_{TRIP} = 1 V	—	0.5	—	µs	

3.2. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	µA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	3.0	—	V	

3.3. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance [1]	$R_{(j-c)Q}$ [2]	1 element operation (IGBT)	—	—	3.6	°C/W	
	$R_{(j-c)F}$ [3]	1 element operation (freewheeling diode)	—	—	4.5	°C/W	

[1] Refers to a case temperature at the measurement point described in Figure 3-1, below.
[2] Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.
[3] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

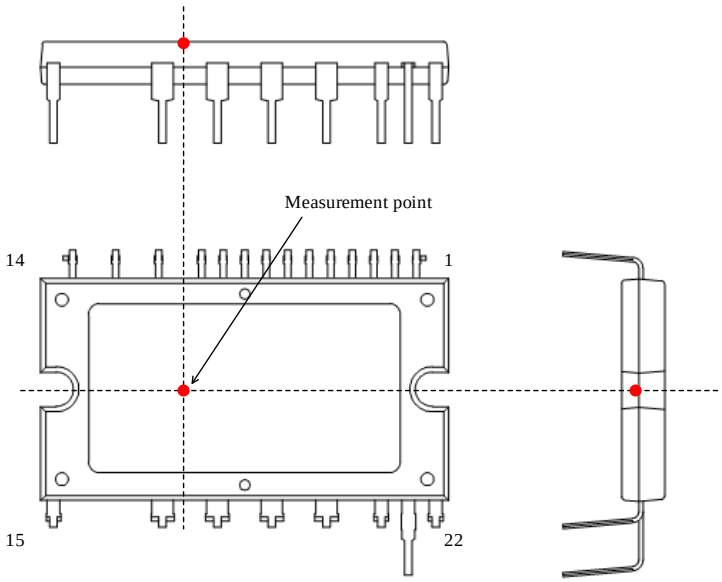


Figure 3-1. Case Temperature Measurement Point

3.4. Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

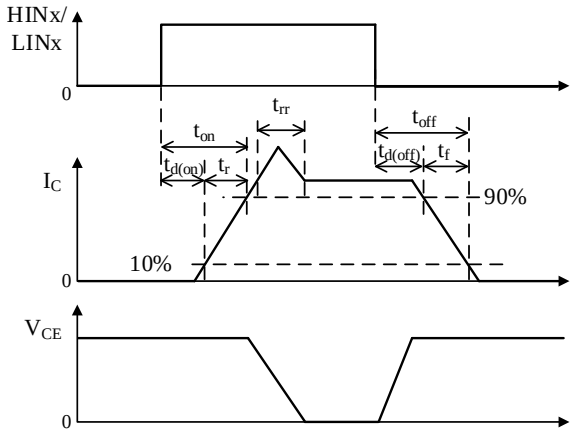


Figure 3-2. Switching Characteristics Definitions

3.4.1. SCM3610C11

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 10 A,V_{IN} = 0 V	—	1.7	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1100	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1000	—	ns
Fall Time	t_f		—	150	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C, inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1060	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1050	—	ns
Fall Time	t_f		—	160	—	ns

3.4.2. SCM3615C11

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 15 A,V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C, inductive load	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1320	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200		ns
Fall Time	t_f		—	140	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C, inductive load	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1320	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200		ns
Fall Time	t_f		—	140	—	ns

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.588	—	0.784	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	100	μm	
Package Weight		—	7.6	—	g	

* When mounting a heatsink, it is recommended to use a metric screw of M3 and a plain washer of 7 mm (φ) together at each end of it. For more details about screw tightening, see Section 13.2.

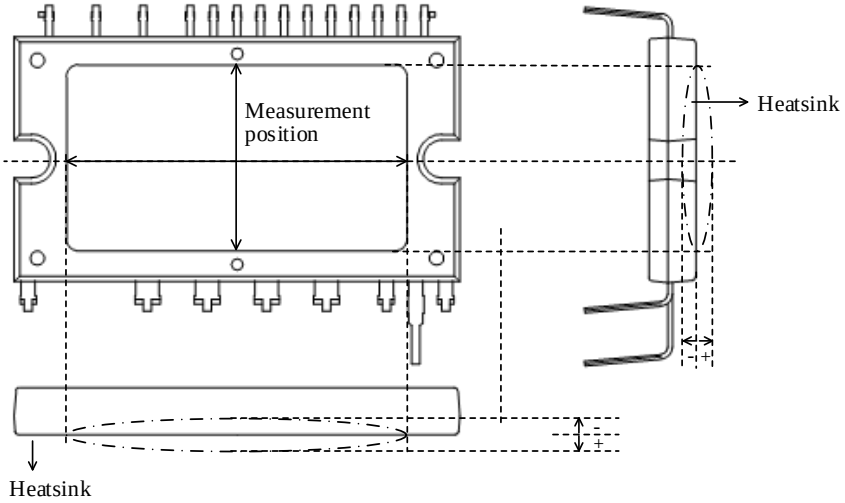


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	2.0	—	—	mm	
Creepage		2.0	—	—	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

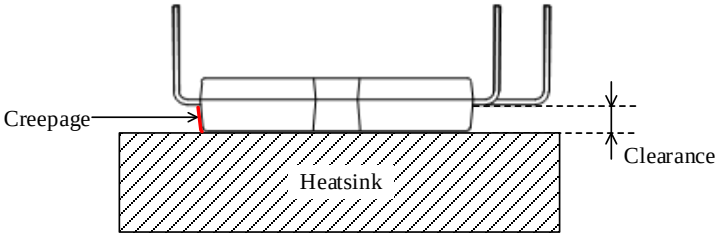


Figure 5-1. Insulation Distance Definitions

6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, the Simultaneous On-state Prevention sets both the high- and low-side transistors off.

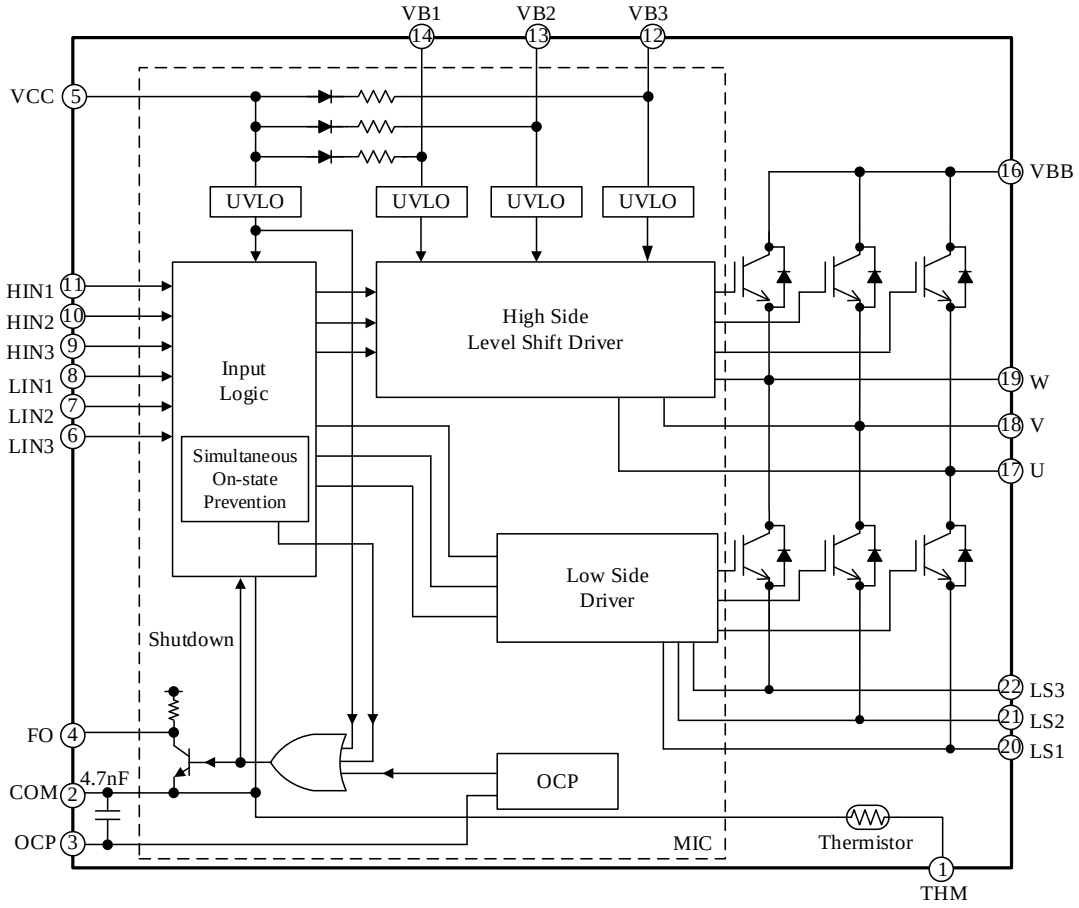
After the IC recovers from a UVLO_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

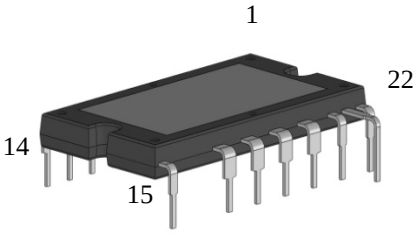
Table 6-1. Truth Table for Operation Modes

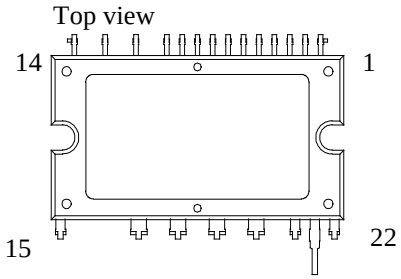
Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF

7. Block Diagram



8. Pin Configuration Definitions





Pin Number	Pin Name	Description
1	THM	Output of thermistor voltage
2	COM	Logic ground
3	OCP	Input for Overcurrent Protection
4	FO	Fault signal output
5	VCC	Input for logic supply voltage
6	LIN3	Logic input for W-phase low-side gate driver
7	LIN2	Logic input for V-phase low-side gate driver
8	LIN1	Logic input for U-phase low-side gate driver
9	HIN3	Logic input for W-phase high-side gate driver
10	HIN2	Logic input for V-phase low-side gate driver
11	HIN1	Logic input for U-phase high-side gate driver
12	VB3	W-phase high-side floating supply voltage input
13	VB2	V-phase high-side floating supply voltage input
14	VB1	U-phase high-side floating supply voltage input
15	NC	(No connection)
16	VBB	Positive DC bus supply voltage
17	U	U-phase output
18	V	V-phase output
19	W	W-phase output
20	LS1	U-phase IGBT emitter
21	LS2	V-phase IGBT emitter
22	LS3	W-phase IGBT emitter

9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

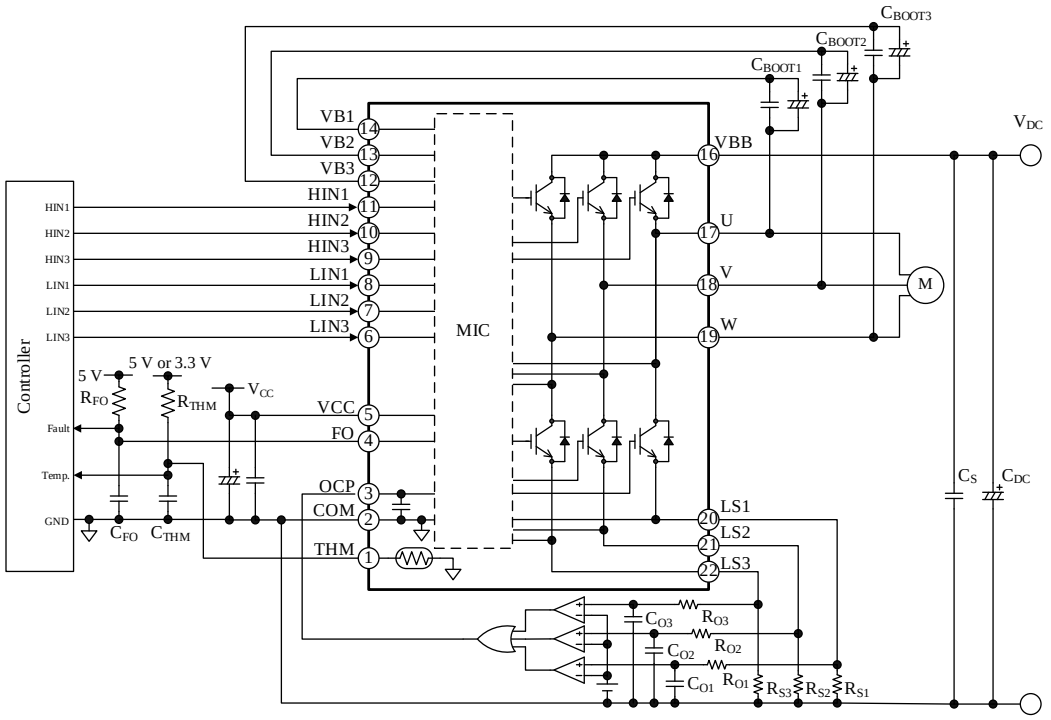


Figure 9-1. Typical Application Using Three Shunt Resistors

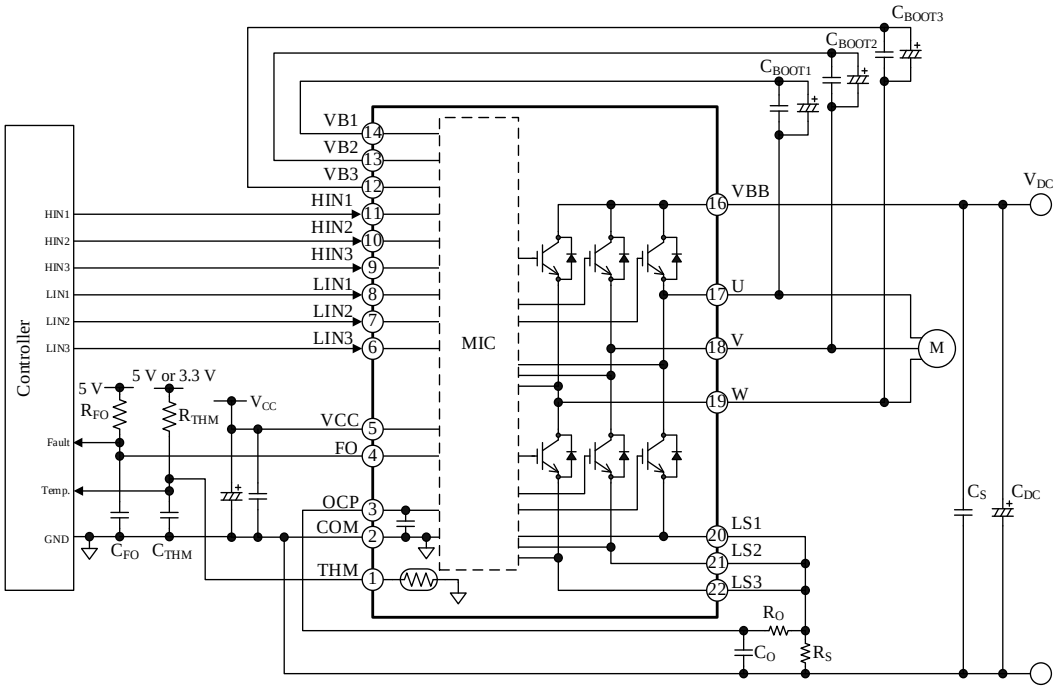
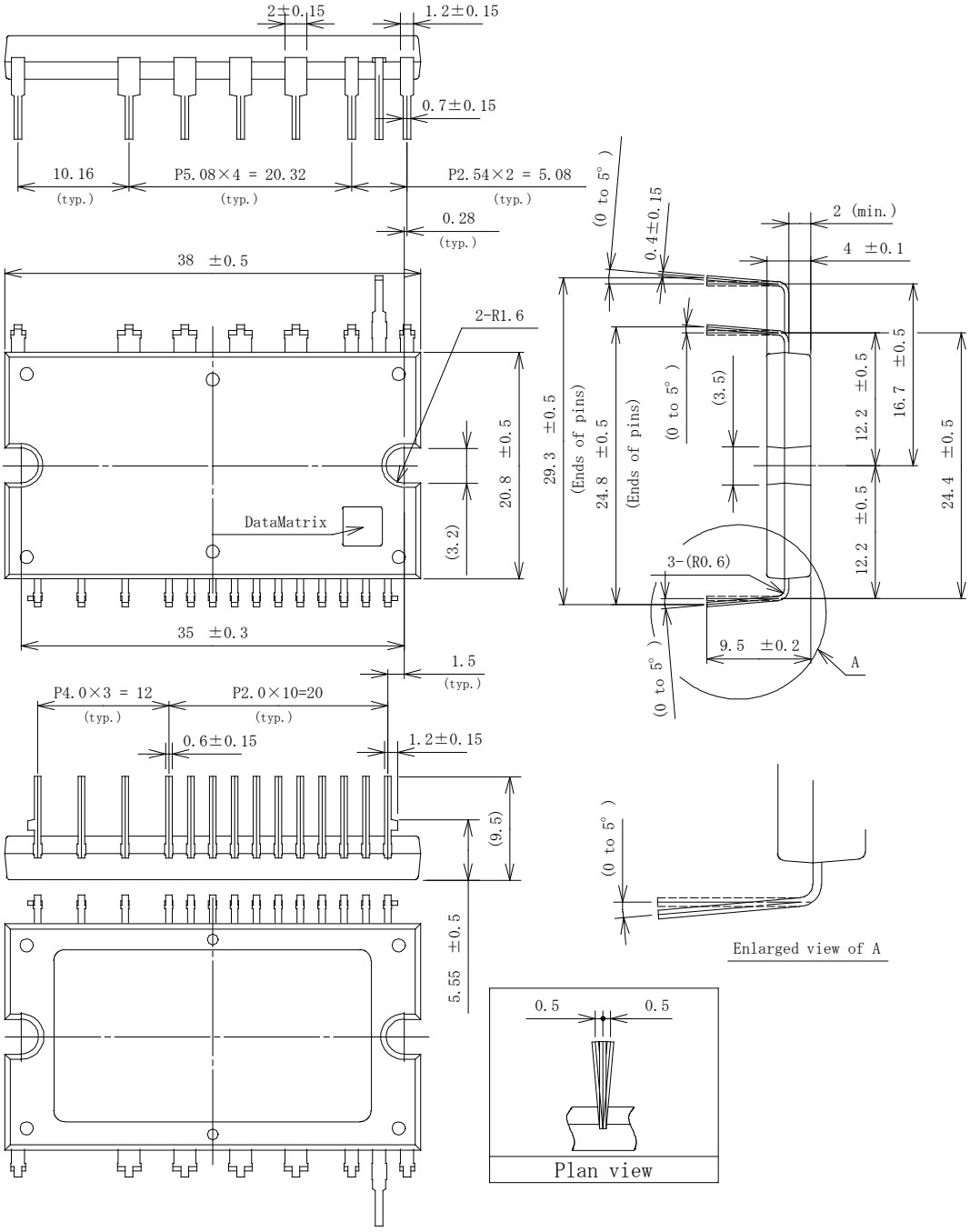


Figure 9-2. Typical Application Using a Single Shunt Resistor

10. Physical Dimensions

10.1. DIP22

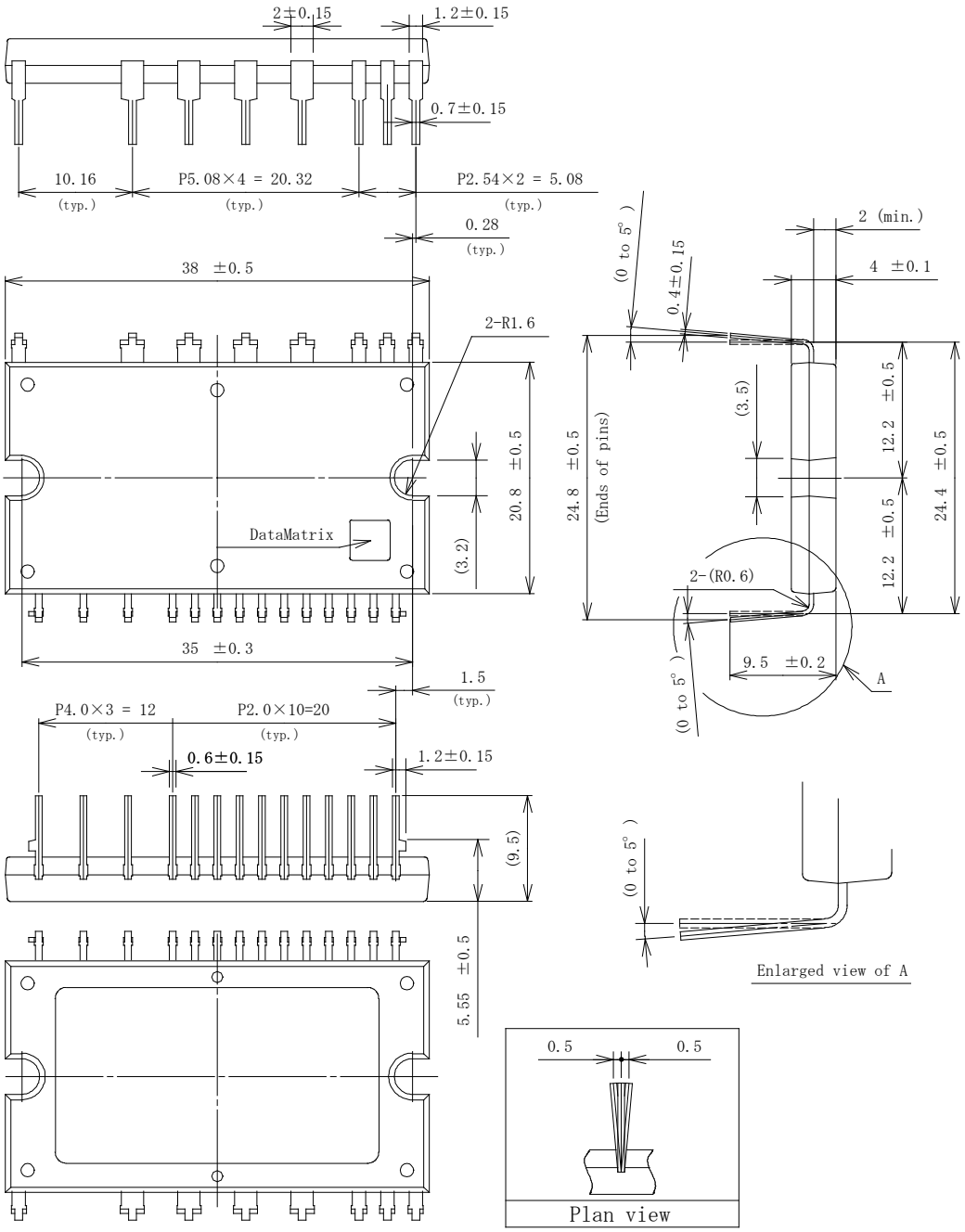
- **Leadform 2581**



NOTES:

- Dimensions in millimeters
- Bare Lead Frame: Pb-free (RoHS compliant)

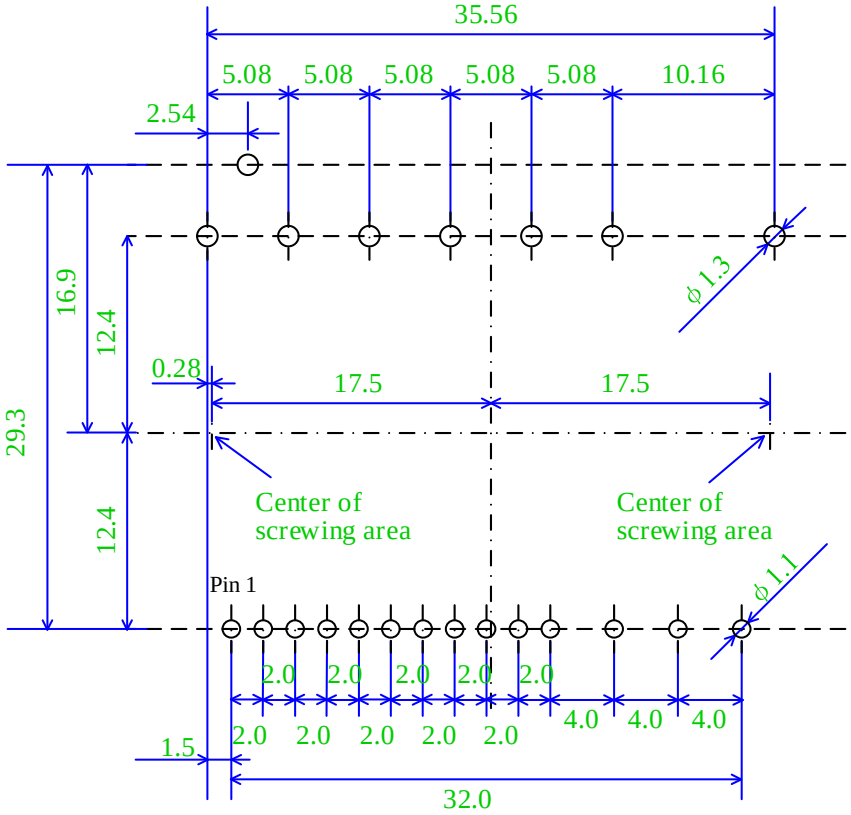
● **Leadform 2582**



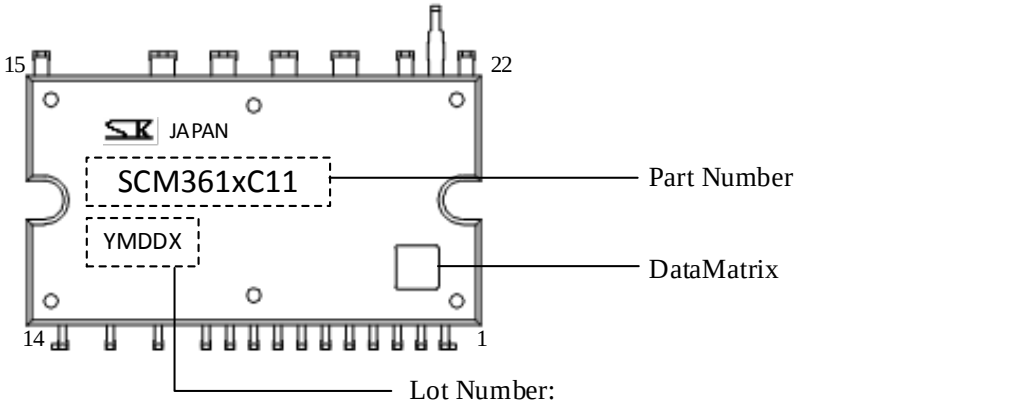
NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)

10.2. Land Pattern Example



11. Marking Diagram



12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

For pin descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x", depending on context. The U-, V-, and W-phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, "the HINx pin" is used when referring to any or all of the HIN1, HIN2, and HIN3 pins.

Also, when different pin names are mentioned as a pair, they are meant to be the pins in the same phase. For example, "the VBx and output (U, V, or W) pins" can be any of "VB1–U", "VB2–V", or "VB3–W".

12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 11.5$ V). It is required to charge bootstrap capacitors, C_{BOOTx}, up to full capacity at startup (see Section 12.2.3).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCC pin voltage.

12.2. Pin Descriptions

12.2.1. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this terminal. Voltages between the VBB and COM pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To absorb surge voltages, put a 0.01 µF to 0.1 µF snubber capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

12.2.2. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor.

These are also the grounds of the high-side floating supplies for each phase, and are connected to the negative nodes of the bootstrap capacitors, C_{BOOTx}.

12.2.3. VCC

This is the logic supply pin for the built-in pre-driver IC. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCC}, near the VCC and COM pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCC and COM pins (as in Figure 12-1).

Voltage to be applied between the VCC and COM pins should be regulated within the recommended operational range of VCC, given in Section 2.

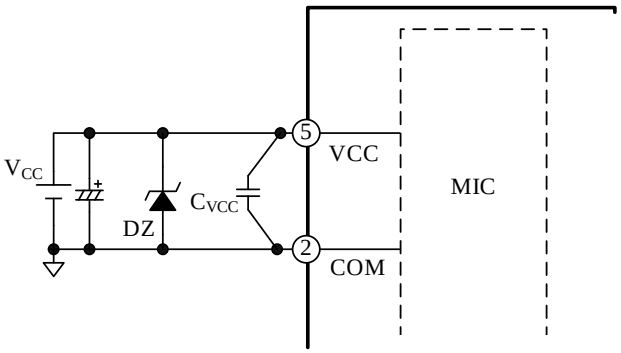


Figure 12-1. VCC Pin and Its Peripheral Circuit

12.2.4. COM

This is the logic ground pin for the built-in pre-driver IC. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to shunt resistors, R_{Sx}, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-2).

Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the COM pin.

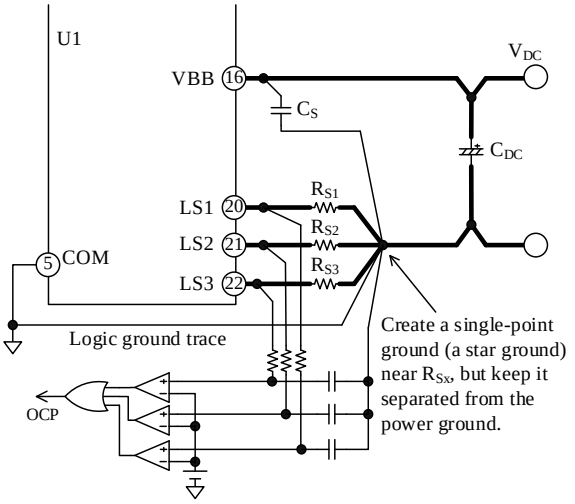


Figure 12-2. Connections to Logic Ground

12.2.5. LS1, LS2, and LS3

These are the emitter pins of the low-side IGBTs. For current detection, the LS1, LS2, and LS3 pins should be connected externally on a PCB via shunt resistors, R_{Sx}, to the COM pin.

When connecting a shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LSx and COM pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RSx}, between the LSx and COM pins in order to prevent the IC from malfunctioning.

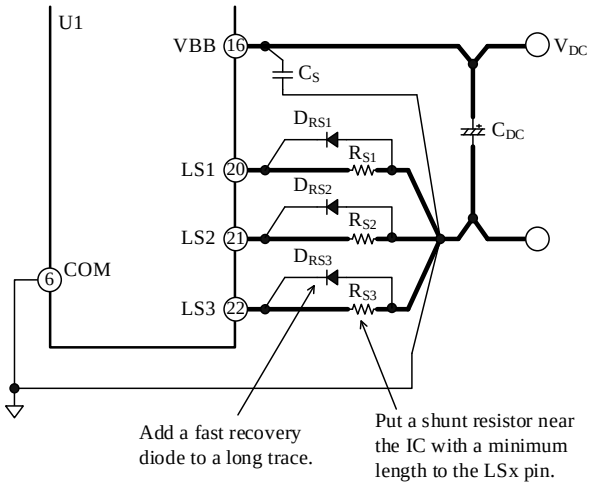


Figure 12-3. Connections to LSx Pin

12.2.6. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases. A bootstrap capacitor, C_{BOOTx}, should be connected in each trace between the VBx and the output (U, V, or W) pins.

Voltages across the VBx and output (U, V, or W) pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

As shown in Figure 12-4, in each trace between VBx and VCC pins, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are placed in series.

For proper startup, turn on the low-side transistor first, then charge the bootstrap capacitor, C_{BOOTx}, up to its maximum capacity. Table 12-1 shows a relation between the charging time and capacitance of C_{BOOTx} at startup.

For capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

$$C_{BOOTx}(\mu F) > 800 \times t_{L(OFF)}\ (s) \quad (1)$$

$$10\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Table 12-1. C_{BOOTx} Capacitance vs. Charging Time at Startup

C_{BOOTx} Capacitance (µF)	Reference Charging Time (s)
10	0.5
22	0.5
47	0.5
100	1.0
220	1.0

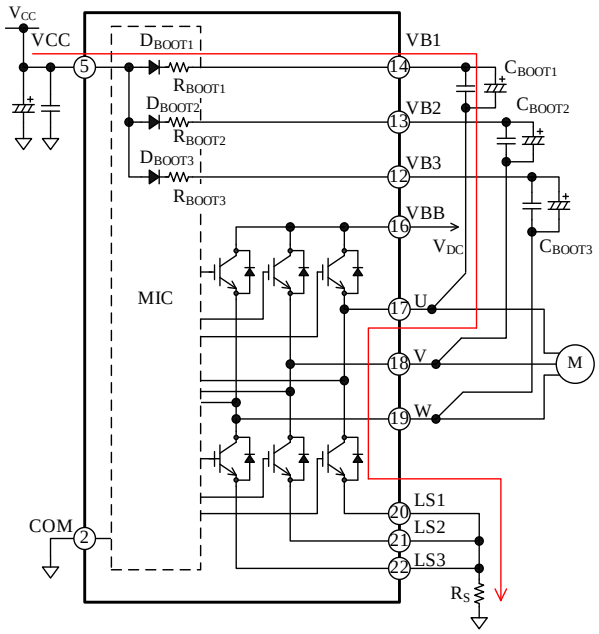


Figure 12-4. Bootstrap Circuit

Even during the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.3.2.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

Figure 12-5 shows an internal level-shifting circuit that produces high-side output signals, HOx. A high-side

output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-6 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output (U, V, or W) pins occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of the high-side output, HOx, stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high, the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition which may result in critical damage to the IC.

To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC, and be connected between the VBx and output (U, V, or W) pins with a minimal length of traces.

To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

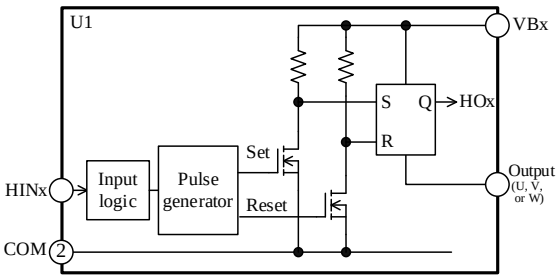


Figure 12-5. Internal Level-shifting Circuit

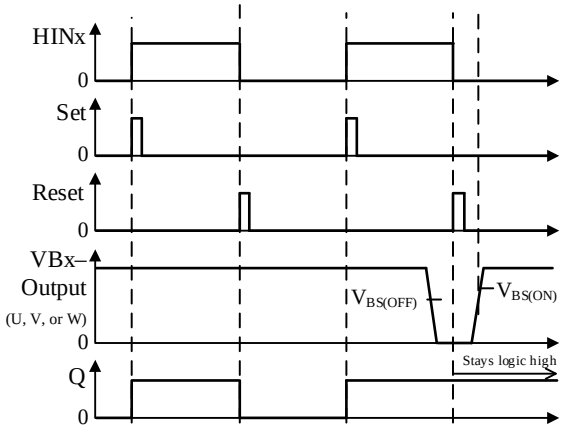


Figure 12-6. Waveforms at VBx–Output Voltage Drop

12.2.7. HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller. Figure 12-7 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 5.5 kΩ pull-down resistor, and its input logic is active high.

Input signals to be applied across the HINx–COM and the LINx–COM pins in each phase should be set within the ranges provided in Table 12-2, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

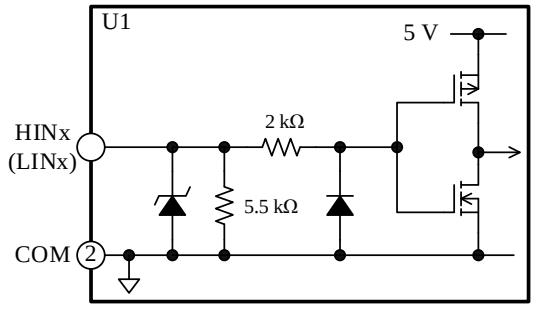


Figure 12-7. Internal Circuit Diagram of HINx or LINx Pin

Table 12-2. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥0.9 µs	

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures can have sufficient margins in the absolute maximum ranges specified in Section 1.

Also, if the traces from the microcontroller to the HINx or LINx pins (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 12-8).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 100 Ω
- R_{IN2x}: 1 kΩ to 10 kΩ
- C_{INx}: 100 pF to 1000 pF

Extra attention should be paid when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected each other,

the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

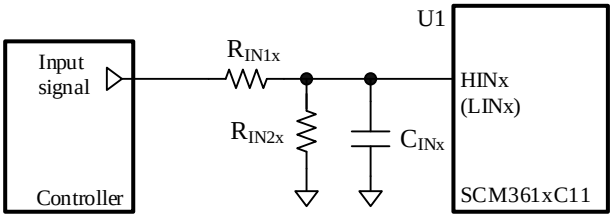


Figure 12-8. Filter Circuit for HINx or LINx Pin

12.2.8. OCP

This pin serves as the input of the Overcurrent Protection (OCP) for monitoring the currents going through the output transistors, with a built-in 4.7 nF ceramic chip capacitor.

Section 12.3.3 provides further information about the OCP circuit configuration and its mechanism.

12.2.9. FO

The FO pin operates as the fault output. Immediately after a fault signal is output from this pin, the microcontroller stops sending input signals to the IC. If you need to resume the motor operation, set the motor to be resumed after a lapse of ≥2 seconds. For more details on this function, see Section 12.3.1.

Figure 12-9 illustrates a schematic diagram of the FO pin and its peripheral circuit. Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage, V_{FO}, should range from 3.0 V to 5.5 V.

Figure 12-10 shows a relation between the FO pin voltage and pull-up resistor, R_{FO}. When the pull-up resistor, R_{FO}, has a too small resistance, the FO pin voltage at fault output becomes high due to the on-resistance of a built-in MOSFET, Q_{FO} (Figure 12-9).

Therefore, it is recommended to use a 1 kΩ to 22 kΩ pull-up resistor when the low-level input threshold voltage of the microcontroller, V_{IL}, is set to 1.0 V.

To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COM pins. Note that, however, this additional filtering allows a delay time, $t_{D(FO)}$, to occur, as seen in Figure 12-11. The delay time, $t_{D(FO)}$, is a period of time which starts when the IC receives a fault flag turning on the internal MOSFET, Q_{FO}, and continues until when the FO pin reaches its threshold voltage (V_{IL}) of 1.0 V or below (put simply, until the time when the IC detects a logic low state, "L"). Figure 12-12 shows how the delay time, $t_{D(FO)}$, and the noise filter capacitor, C_{FO}, are related. To avoid the repetition of Overcurrent Protection (OCP) activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the internal MOSFET (Q_{FO}) turn-on. t_P is 15 µs where minimum values of thermal characteristics are taken into account. (For more details, see Section 12.3.3.) When V_{IL} is set to 1.0 V, it is recommended to use a 0.001 µF to 0.01 µF noise filter capacitor, C_{FO}, allowing a sufficient margin to deal with variations in characteristics.

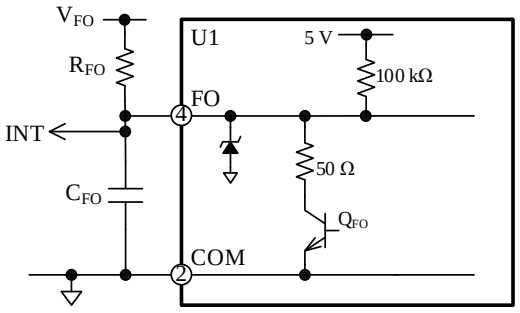


Figure 12-9. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

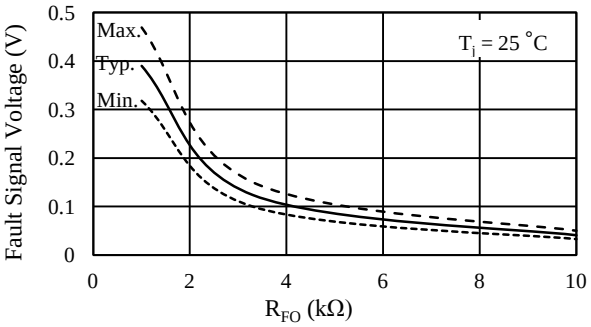


Figure 12-10. Fault Signal Voltage vs. Pull-up Resistor, R_{FO}

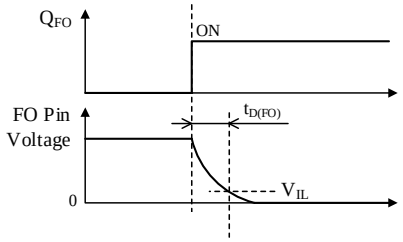


Figure 12-11. FO Pin Delay Time, $t_{D(FO)}$

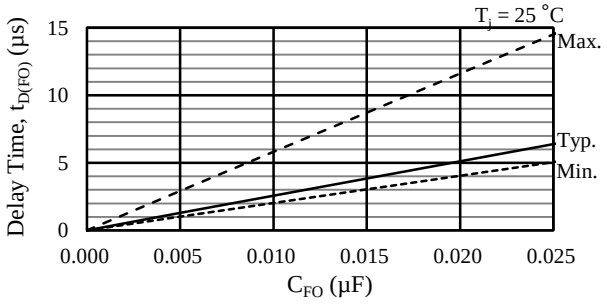


Figure 12-12. Delay Time, $t_{D(FO)}$ vs. Filter Capacitor, C_{FO}

12.2.10. THM

The SCM3000C series incorporates a built-in thermistor for case temperature detection. The THM pin operates as the output of the thermistor voltage which monitors the case temperature of the IC via the external microcontroller.

The SCM3000C series does not have any protection against overtemperature; therefore, the motor must be externally controlled when a temperature rise occurs, or be controlled with such protective measures.

Moreover, note that the THM pin output does not provide the temperature followability, especially when a rapid temperature rise in the output transistors occurs during motor lock and short circuit conditions.

When connecting a thermistor, connect one end of it to the THM pin, then internally connect the other end to the COM pin. Figure 12-14 depicts a typical thermistor resistance vs. temperature curve; Figure 12-15 plots a typical performance curve of the THM pin.

The THM pin should be tied to the external power supply, along with a pull-up resistor, R_{THM}, and a noise filter capacitor, C_{THM}.

For proper IC operation, you application must be set as follows: The external power supply voltage, V_{THM}, should range from 3.0 V to 5.5 V. Use R_{THM} with a resistance of ≥4.4 kΩ, and C_{THM} with a capacitance of ≥4.7 nF. Then, place C_{THM} as close as possible to the IC with minimizing a trace length between the THM and COM pins.

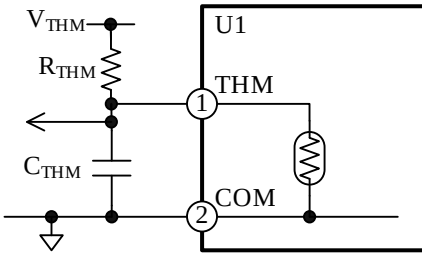


Figure 12-13. Internal Circuit Diagram of THM Pin and Its Peripheral Circuit

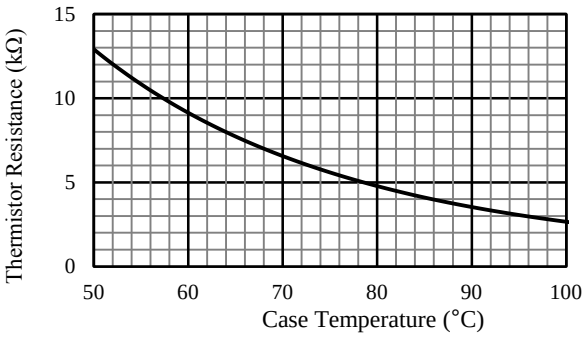


Figure 12-14. Typical Thermistor Resistance vs. Temperature Curve

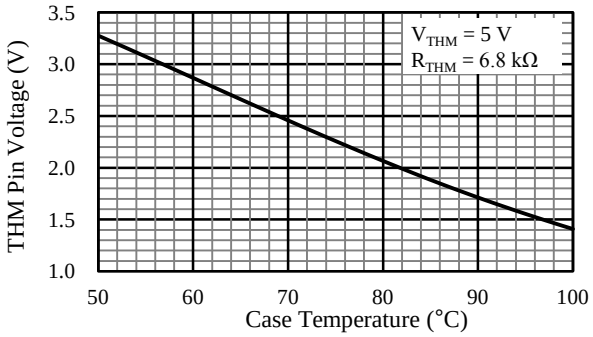


Figure 12-15. THM Pin Typical Performance Curve

12.3. Protection Functions

This section describes the various protection circuits provided in the SCM3000C series. The protection circuits include: the Undervoltage Lockout for power supplies (UVLO), the Simultaneous On-state prevention, and the Overcurrent Protection (OCP).

In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor (see also the diagram in Section 7).

12.3.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (≤0.5 V).

1) Low-side Undervoltage Lockout (UVLO_VCC)
2) Overcurrent Protection (OCP)
3) Simultaneous On-state Prevention

During the time when the FO pin holds the logic low state, the high- and low-side transistors of all phases turn off. In normal operation, the FO pin holds a logic high state and outputs a 5 V signal. The fault signal output time of the FO pin at OCP activation is the OCP hold time (t_P) of 30 µs (typ.), fixed by a built-in feature of the IC itself (see Section 12.3.3). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P. If you need to resume the motor operation, set the motor to be resumed after a lapse of ≥2 seconds.

12.3.2. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SCM3000C series has the Undervoltage Lockout (UVLO) circuits for both of the high- and low-side power supplies in the monolithic IC (MIC).

12.3.2.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-16 shows operational waveforms of the undervoltage lockout operation for high-side power supply (i.e., UVLO_VB).

When the voltage between the VBx and output (U, V, or W) pins decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$, 10 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low.

When the voltage between the VBx and output (U, V, or W) pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$, 10.5 V) or more, the IC releases the UVLO_VB condition. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release. The FO pin does not transmit any fault signals during the UVLO_VB is in operation.

In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

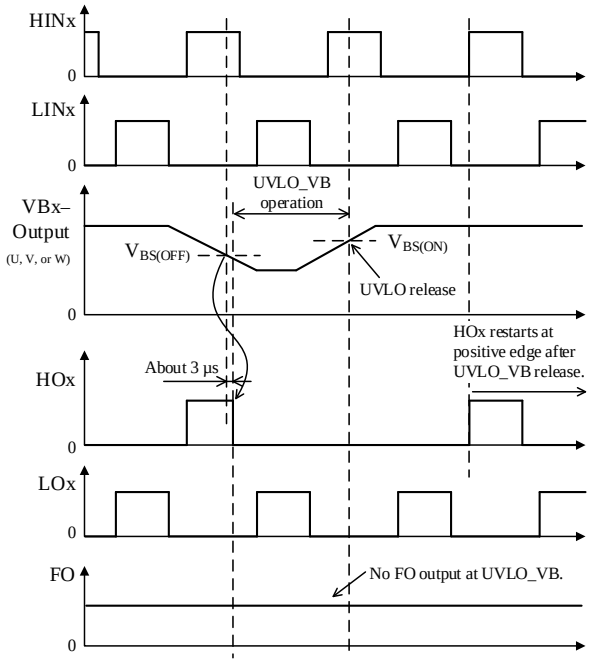


Figure 12-16. Operational Waveforms of UVLO_VB

12.3.2.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-17 shows operational waveforms of the undervoltage lockout operation for low-side power supply (i.e., UVLO_VCC). When the VCC pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$, 10 V) or less, the UVLO_VCC circuit in the corresponding phase activates and sets both of HOx and LOx signals to logic low.

When the VCC pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$, 10.5 V) or more, the IC releases the UVLO_VCC condition. Then it resumes transmitting the HOx and LOx signals according to input commands on the HINx and LINx pins.

During the UVLO_VCC operation, the FO pin becomes logic low and sends fault signals. In addition, the VCC pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

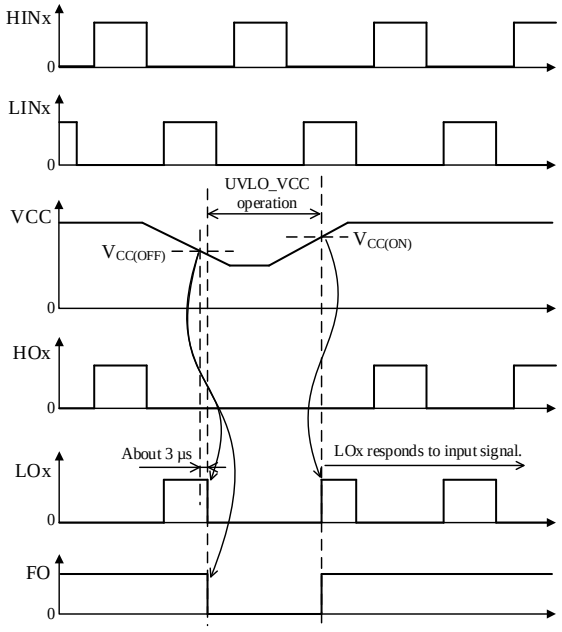


Figure 12-17. Operational Waveforms of UVLO_VCC

12.3.3. Overcurrent Protection (OCP)

Figure 12-18 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with the input voltages across external shunt resistors, R_{Sx}. Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_{Sx}.

Figure 12-19 is a timing chart that represents operation waveforms during OCP operation. When the OCP pin voltage increases to the Overcurrent Protection Threshold Voltage (V_{TRIP}, 0.500 V) or more, and remains in this condition for a period of the Overcurrent Protection Blanking Time (t_{BK}, 0.5 µs) or longer, the OCP is activated. The enabled OCP circuit then shuts off the output transistors and puts the FO pin into a logic low state. And output current decreases after the output transistors turn off. Even if the OCP pin voltage falls below V_{TRIP}, the IC holds the FO pin the logic low state for a fixed OCP hold time (t_P) of 30 µs (typ.). Then, the output transistors operate according to input signals.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. When putting the IC back to normal operation, you must set up a wait time of 2 seconds or longer before resuming the IC operation.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor a recommended resistance, R_{Sx} (see Section 2).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 2).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_{Sx}. In addition, choose a resistor with allowable power dissipation according to your application.

As illustrated in Figure 12-18, a 4.7 nF chip capacitor, C_{OIN}, is internally connected to the OCP pin. When you connect a CR filter (i.e., a pair of a filter resistor, R_O, and a filter capacitor, C_O) to the OCP pin, care should be taken in setting the time constants of R_O, C_O, and C_{OIN}. The larger the time constant, the longer the time that the OCP pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their values should satisfy Equation (3):

$$R_O \times (C_O + 4.7\ \text{nF}) < 1.0\ \mu\text{s}. \quad (3)$$

It is recommended to use R_O with a resistance up to 200 Ω and C_O with a capacitance of about 4.7 nF. And place C_O as close as possible to the IC with minimizing a trace length between the OCP and COM pins.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

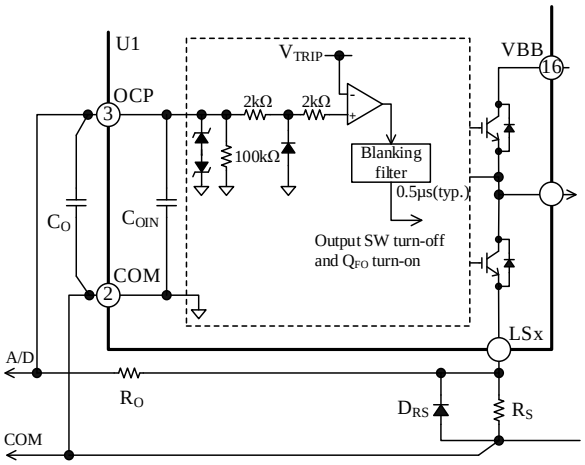


Figure 12-18. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

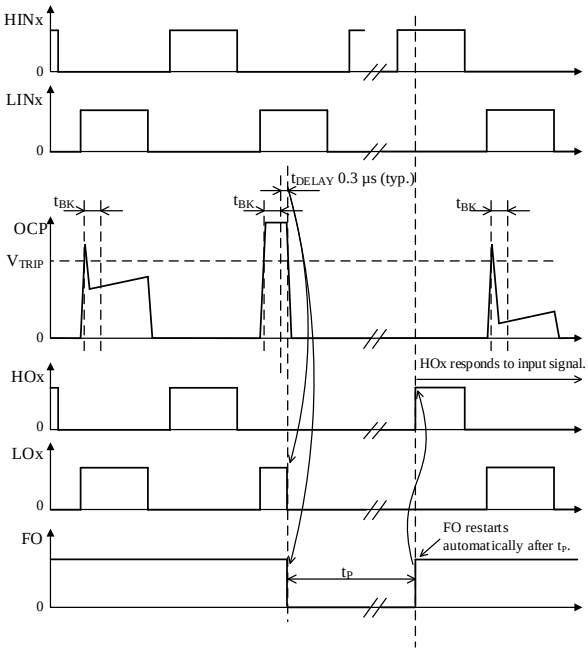


Figure 12-19. OCP Operational Waveforms

12.3.4. Simultaneous On-state Prevention

In case both of the HINx and LINx pins receive logic high signals at once, the high- and low-side transistors turn on at the same time, allowing overcurrents to pass through. As a result, the switching transistors will be destroyed. To prevent this event, the Simultaneous On-state Prevention circuit is built into the SCM3000C series. Note that incorrect command input and noise interference are also largely responsible for such a simultaneous-on condition.

When logic high signals are asserted on the HINx and LINx pins at once, as in Figure 12-20, this function gets activated and turns the high- and low-side transistors off. Then, during the function is being enabled, the FO pin becomes logic low and sends fault signals. After the IC comes out of the simultaneous on-state condition, "HOx" and "LOx" start responding in accordance with HINx and LINx input commands again.

To prevent noise-induced malfunctions, the Simultaneous On-state Prevention circuit has a filter of about 0.8 µs. Note that this function does not have any of dead-time programming circuits. Therefore, input signals to the HINx and LIN pins must have proper dead times as defined in Section 12.2.7.

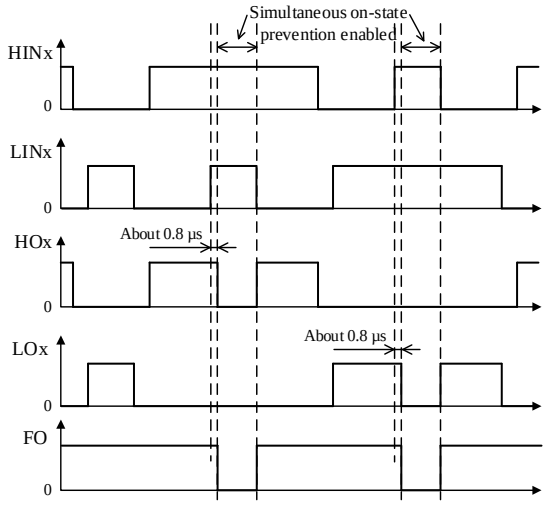


Figure 12-20. Operational Waveforms of Simultaneous On-state Prevention

13. Design Notes

This section also employs the notation system described in the beginning of the previous section.

13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths carrying high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which carry high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

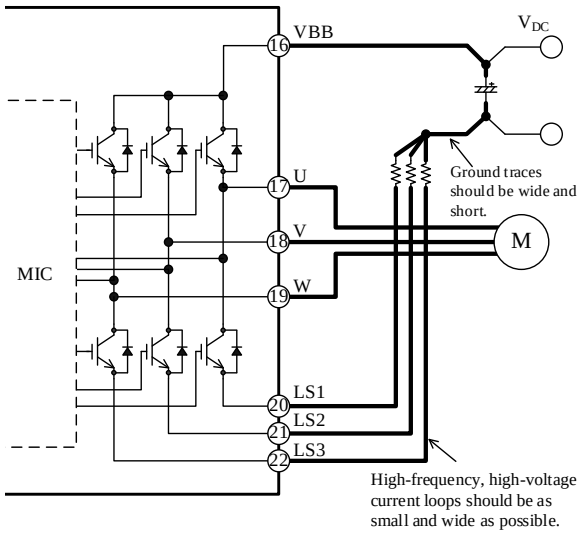


Figure 13-1. High-frequency, High-voltage Current Paths

13.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a pair of a metric screw of M3 and a plain washer of 7 mm (φ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally-conductive sheet or an electrically insulating sheet is used, package cracks

may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.

- When applying a silicone grease, make sure that there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 µm
  - Heatsink flatness: ±100 µm
  - Apply silicone grease within the area indicated in Figure 13-2, below.

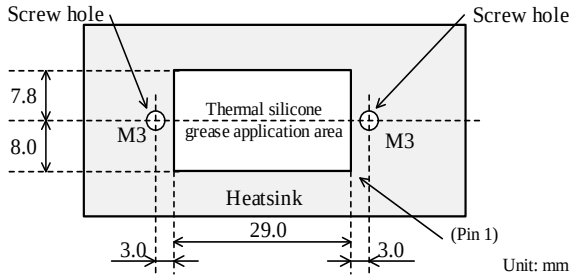


Figure 13-2. Reference Application Area for Thermal Silicone Grease

13.3. Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that all of the output (U, V, and W), LSx, and COM pins must be appropriately connected. Otherwise the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{1H}) in the U phase; Figure 13-4 shows the low-side transistor (Q_{1L}) in the U phase.

When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LSx pin to be measured to the COM pin, then leave other unused pins open.

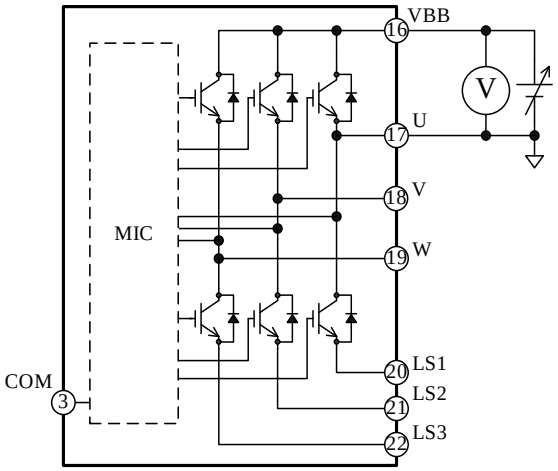


Figure 13-3. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

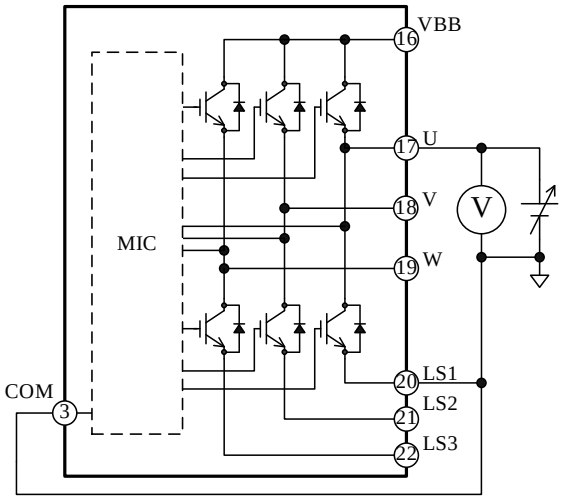


Figure 13-4. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

14. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate junction temperature. Note that the descriptions listed here are applicable to the SCM3000C series, which is controlled by a 3-phase sine-wave PWM driving strategy. Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT00xx: SCM3000C Series Calculation Tool
  http://www.semicon.sanken-ele.co.jp/calc-tool/scm3xxxc_caltool_jp.html

14.1. IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 15.3.1.

As expressed by the curves in Figure 14-1, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)} - I_C$ curve, and
β is the slope of the linear approximation in the $V_{CE(SAT)} - I_C$ curve.

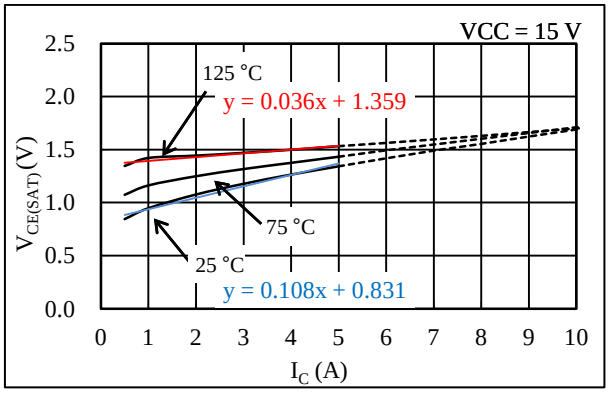


Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)} - I_C$ Curve

14.2. IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (5)$$

Where:

fc is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope of the switching loss curve (see Section 15.3.2).

14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, Tj, can be estimated with Equation (6):

$$T_j = R_{(j-C)Q} \times (P_{ON} + P_{SW}) + T_C . \quad (6)$$

Where:

$R_{(j-c)Q}$ is the junction-to-case thermal resistance per IGBT (°C/W), and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

15. Performance Curves

15.1. Transient Thermal Resistance Curves

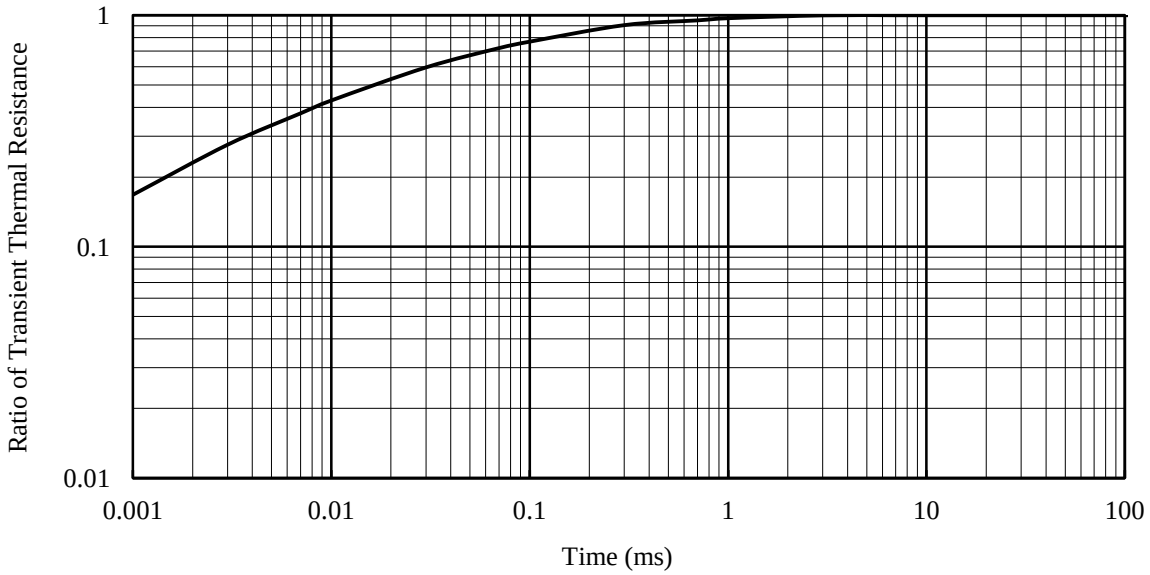


Figure 15-1. SCM3610C11 Transient Thermal Resistance Curve

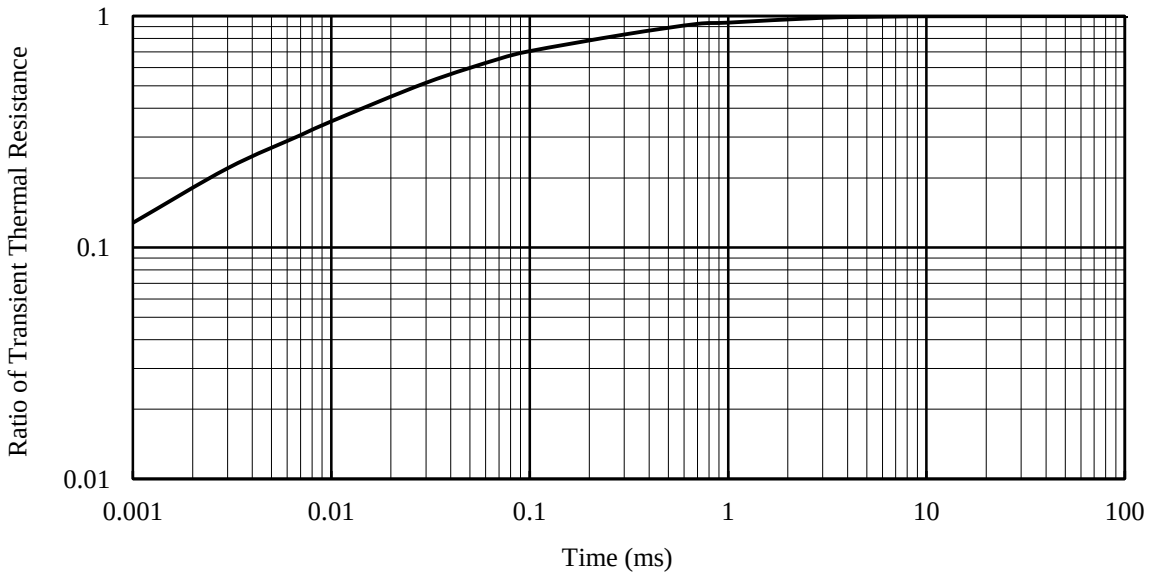


Figure 15-2. SCM3615C11 Transient Thermal Resistance Curve

15.2. Performance Curves of Control Parts

Figure 15-3 to Figure 15-23 provide performance curves of the control parts integrated in the SCM3000C series, including variety-dependent characteristics and thermal characteristics. T_j represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-3	Logic Supply Current, I_{CC} vs. T_C
Figure 15-4	Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}
Figure 15-5	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 15-6	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 15-7	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B
Figure 15-8	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-9	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-10	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-11	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-12	UVLO_VB Filtering Time vs. T_C
Figure 15-13	UVLO_VCC Filtering Time vs. T_C
Figure 15-14	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 15-15	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-16	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 15-17	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-18	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-19	FO Pin Voltage in Normal Operation, V_{FOL} vs. T_C
Figure 15-20	Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-21	Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C
Figure 15-22	Overcurrent Protection Hold Time, t_P vs. T_C
Figure 15-23	Filtering Time of Simultaneous On-state Prevention vs. T_C

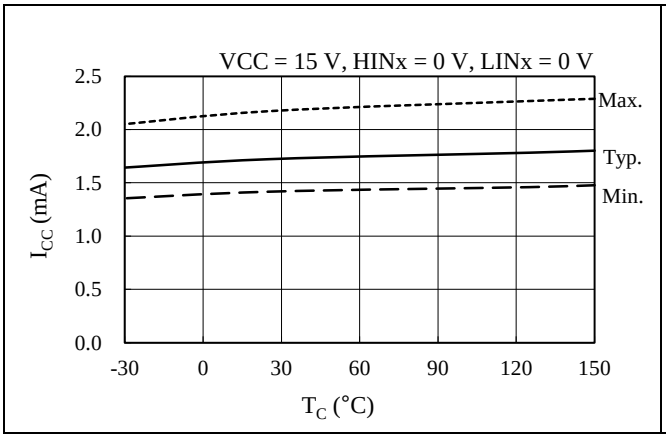


Figure 15-3. Logic Supply Current, I_{CC} vs. T_C

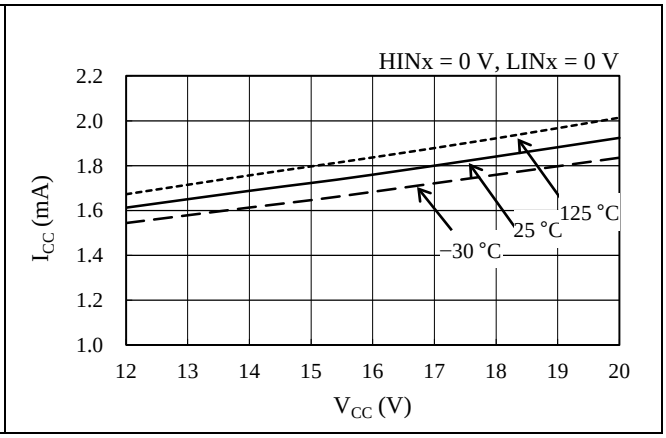


Figure 15-4. Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}

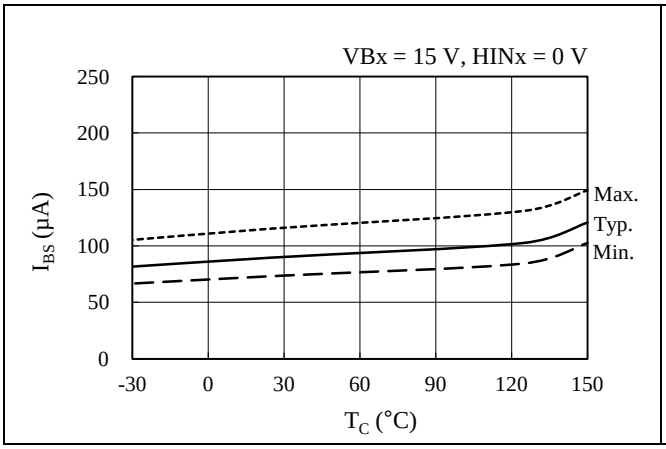


Figure 15-5. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

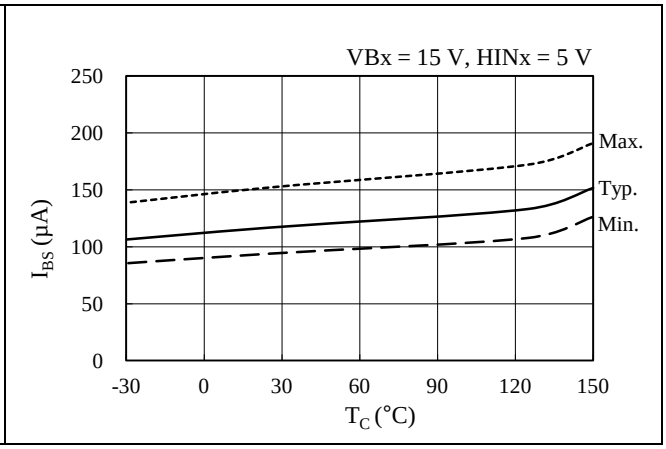


Figure 15-6. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

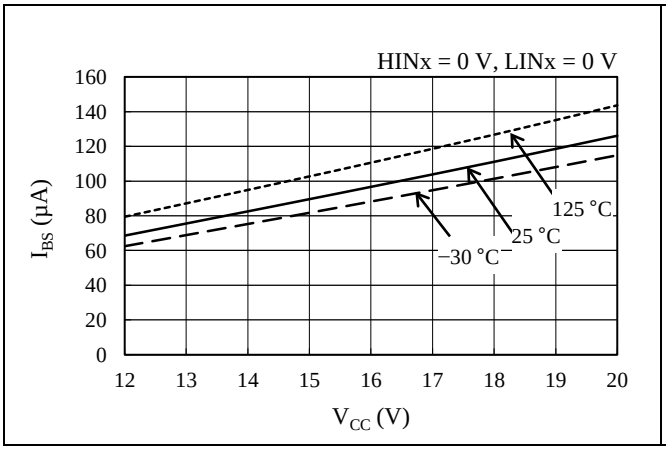


Figure 15-7. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B

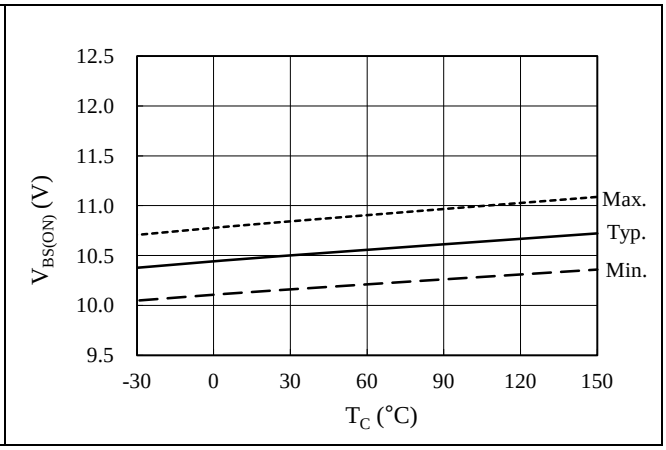


Figure 15-8. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

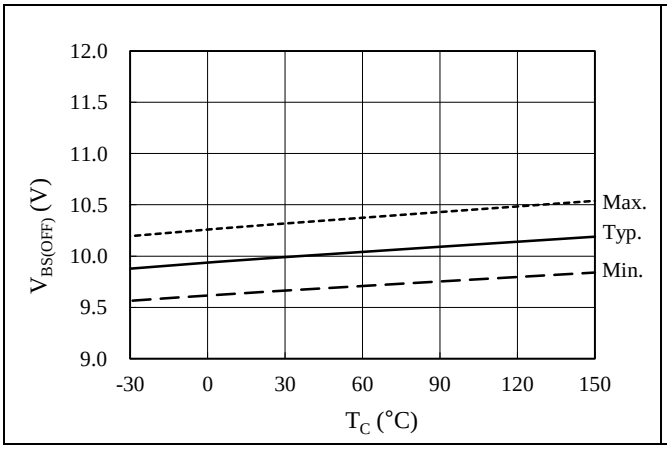


Figure 15-9. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

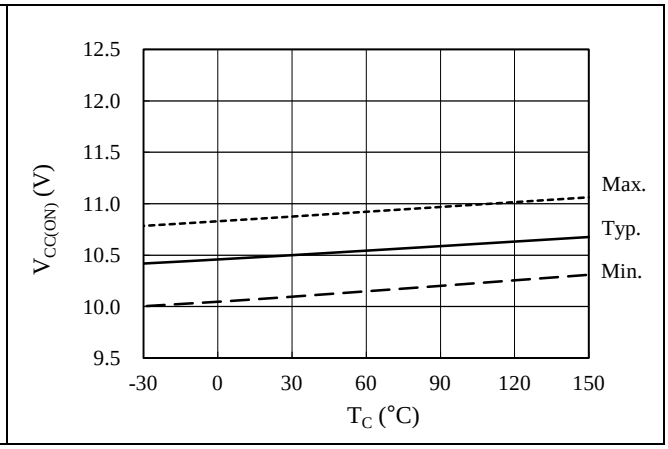


Figure 15-10. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

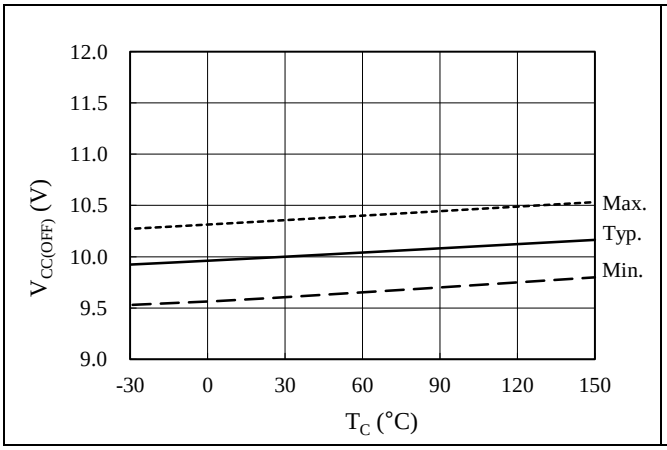


Figure 15-11. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

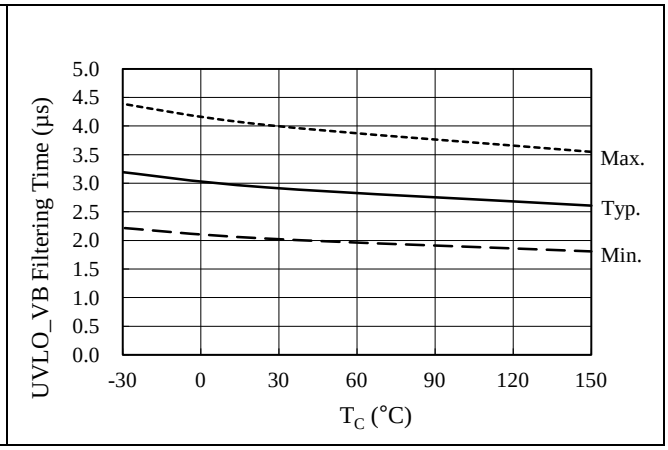


Figure 15-12. UVLO_VB Filtering Time vs. T_C

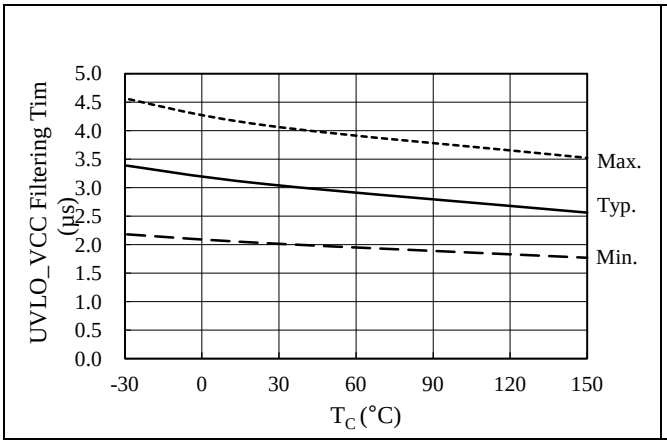


Figure 15-13. UVLO_VCC Filtering Time vs. T_C

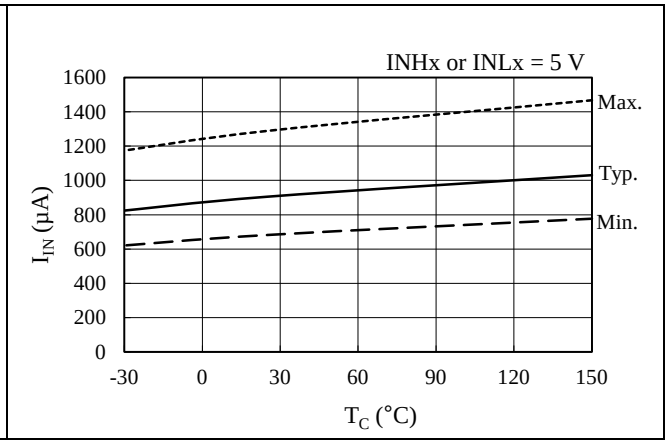


Figure 15-14. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

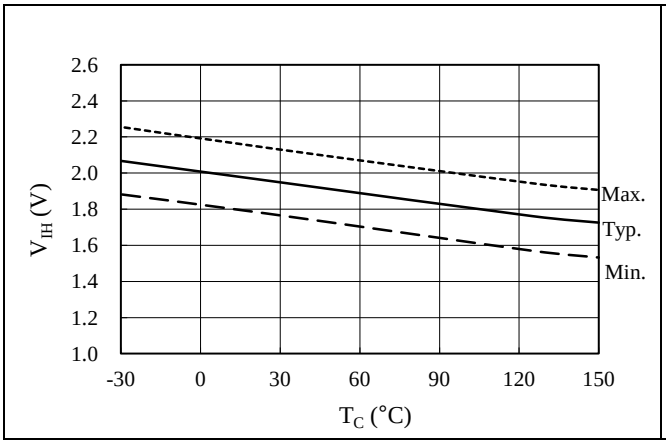


Figure 15-15. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

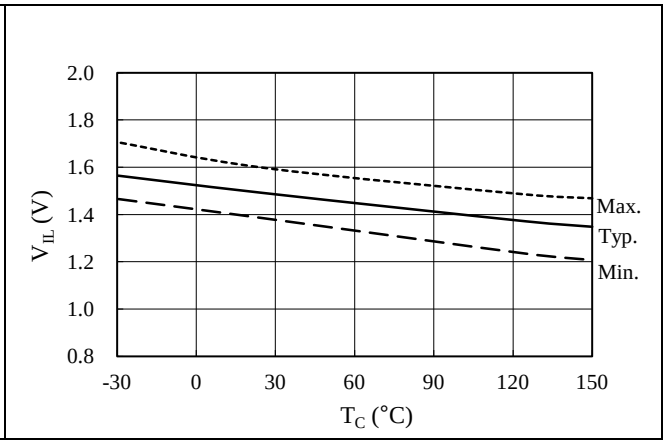


Figure 15-16. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

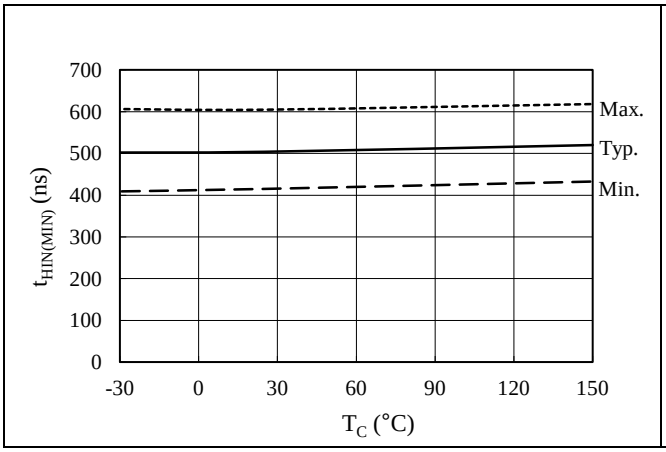


Figure 15-17. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

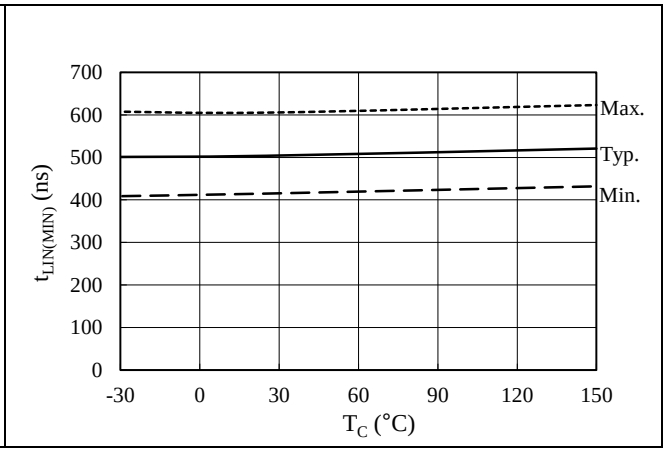


Figure 15-18. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

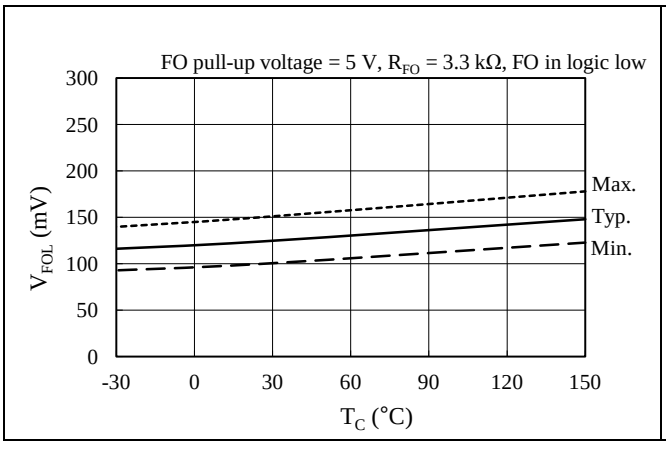


Figure 15-19. FO Pin Voltage in Normal Operation, V_{FOL} vs. T_C

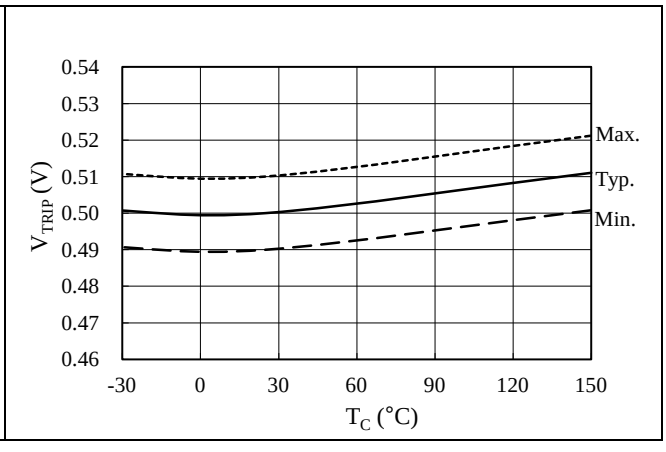


Figure 15-20. Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C

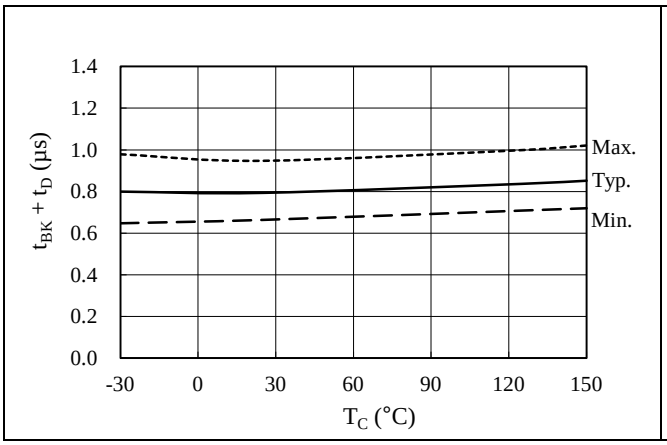


Figure 15-21. Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C

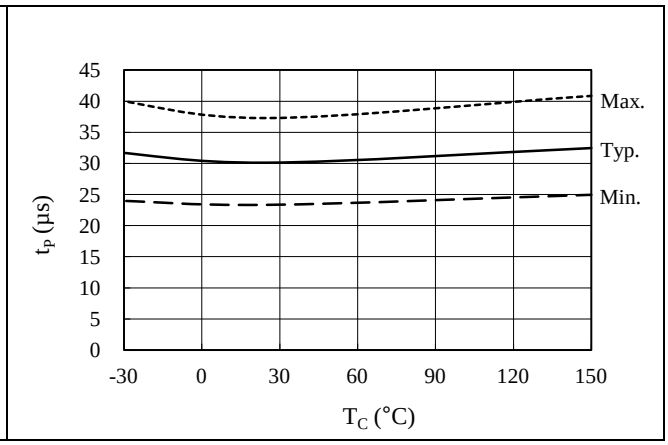


Figure 15-22. Overcurrent Protection Hold Time, t_P vs. T_C

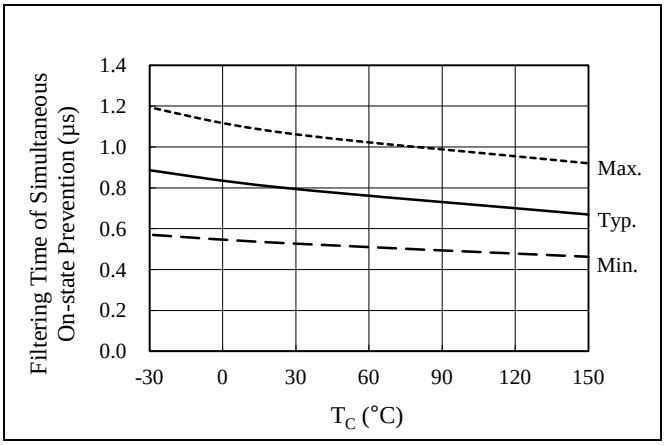


Figure 15-23. Filtering Time of Simultaneous On-state Prevention vs. T_C

15.3. Performance Curves of Output Parts

15.3.1. Output Transistor Performance Curves

15.3.1.1. SCM3610C11

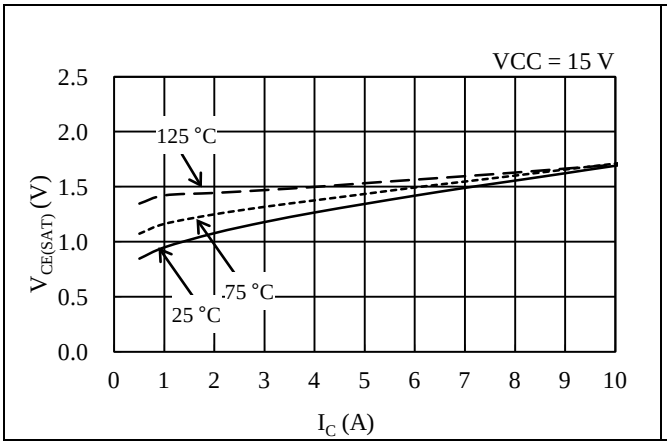


Figure 15-24. IGBT $V_{CE(SAT)}$ vs. I_C

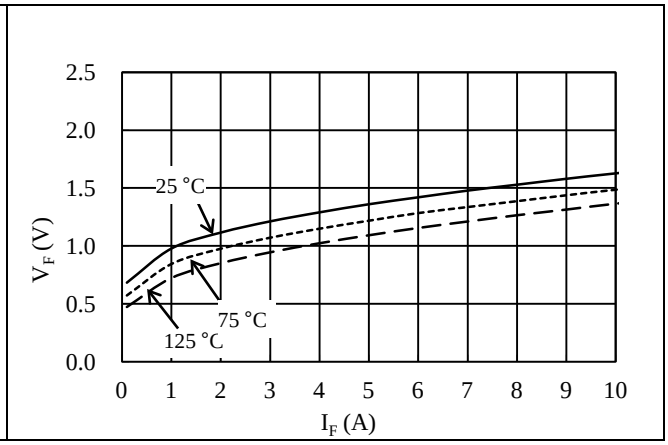


Figure 15-25. Freewheeling Diode V_F vs. I_F

15.3.1.2. SCM3615C11

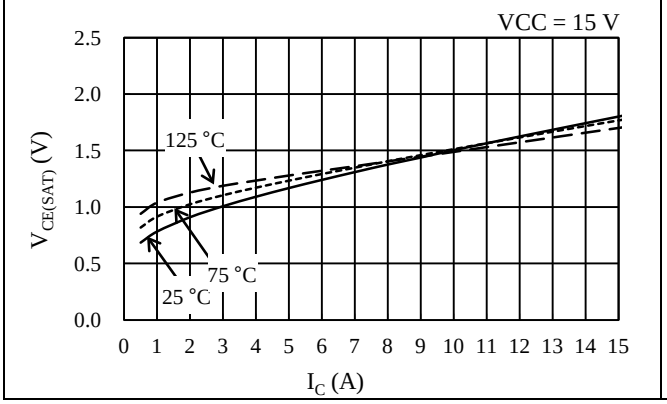


Figure 15-26. IGBT VCE(SAT) vs. IC

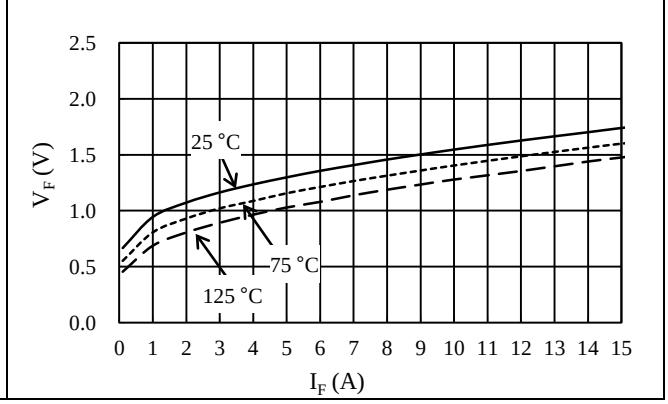


Figure 15-27. Freewheeling Diode VF vs. IF

15.3.2. Switching Losses

Conditions: VBB = 300 V, half-bridge circuit with inductive load.

15.3.2.1. SCM3610C11

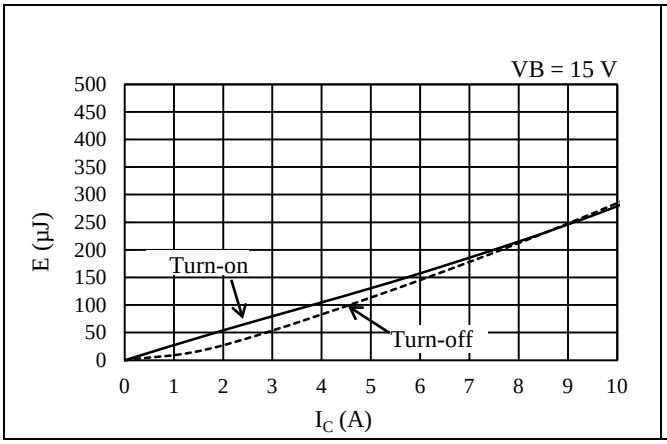


Figure 15-28. High-side Switching Loss (T_j = 25 °C)

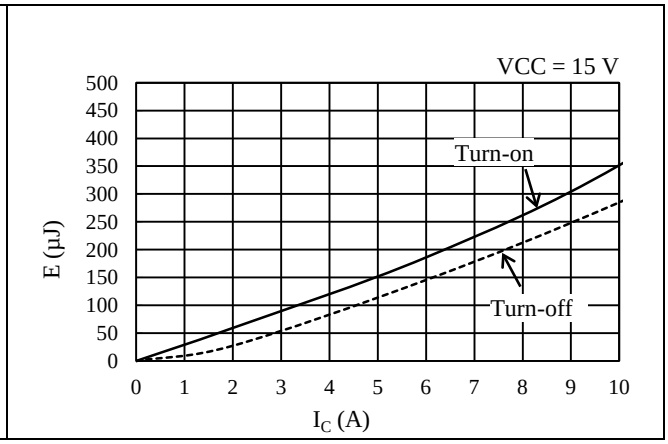


Figure 15-29. Low-side Switching Loss (T_j = 25 °C)

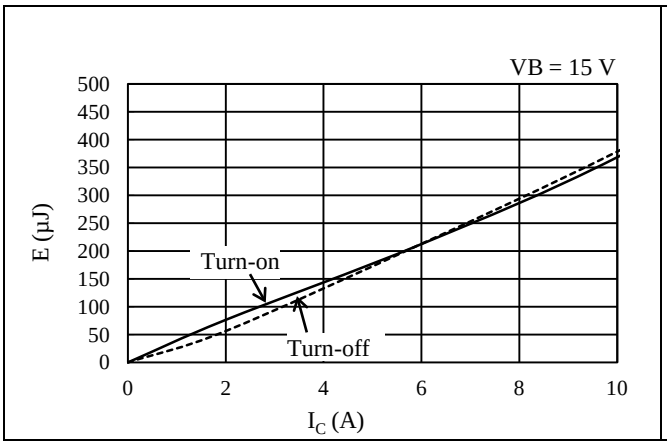


Figure 15-30. High-side Switching Loss (T_j = 125 °C)

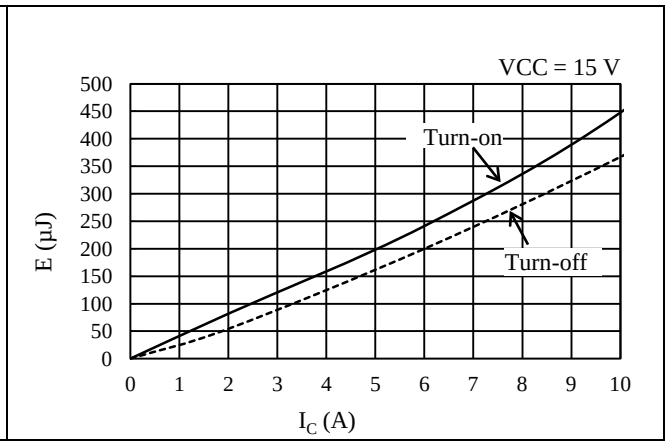


Figure 15-31. Low-side Switching Loss (T_j = 125 °C)

15.3.2.2. SCM3615C11

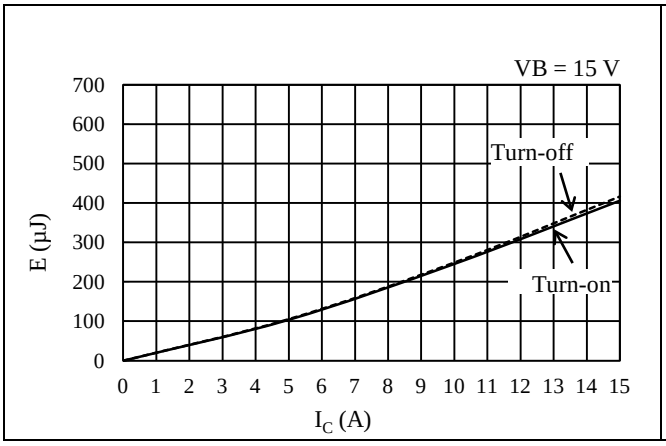


Figure 15-32. High-side Switching Loss (Tj = 25 °C)

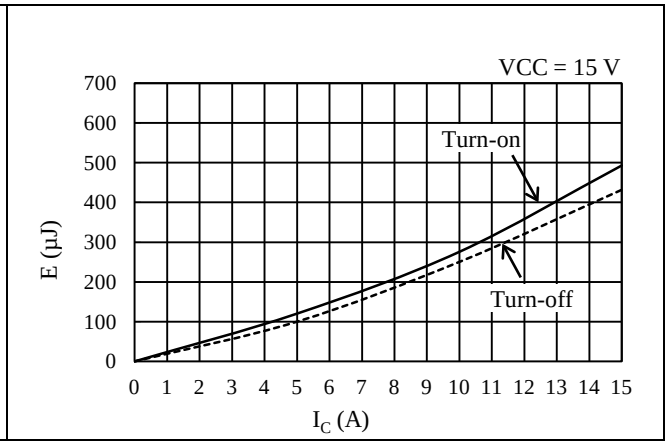


Figure 15-33. Low-side Switching Loss (T_j = 25 °C)

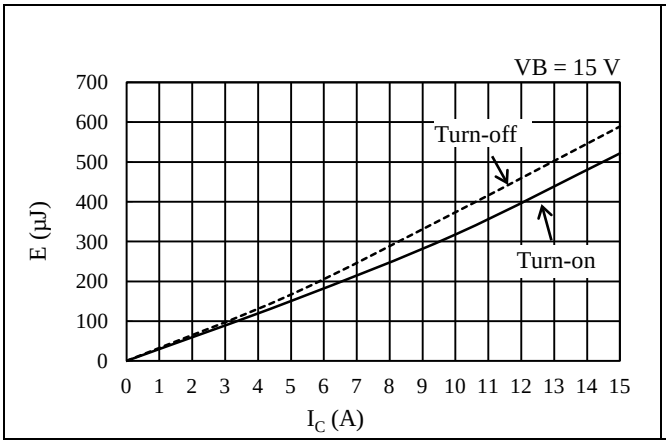


Figure 15-34. High-side Switching Loss (T_j = 125 °C)

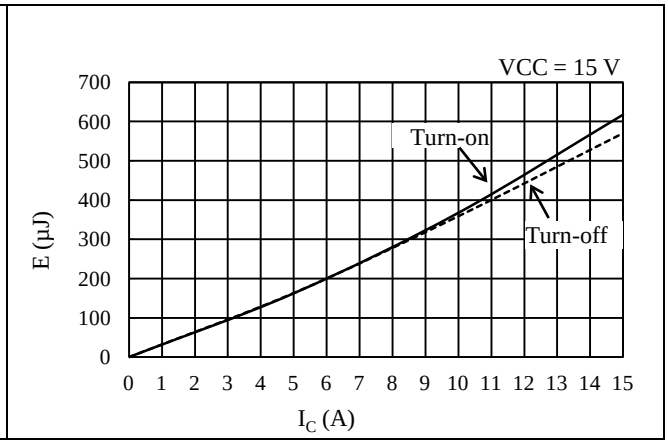


Figure 15-35. Low-side Switching Loss (T_j = 125 °C)

15.4. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $V_{CE(SAT)}$ and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_j = 150 °C.

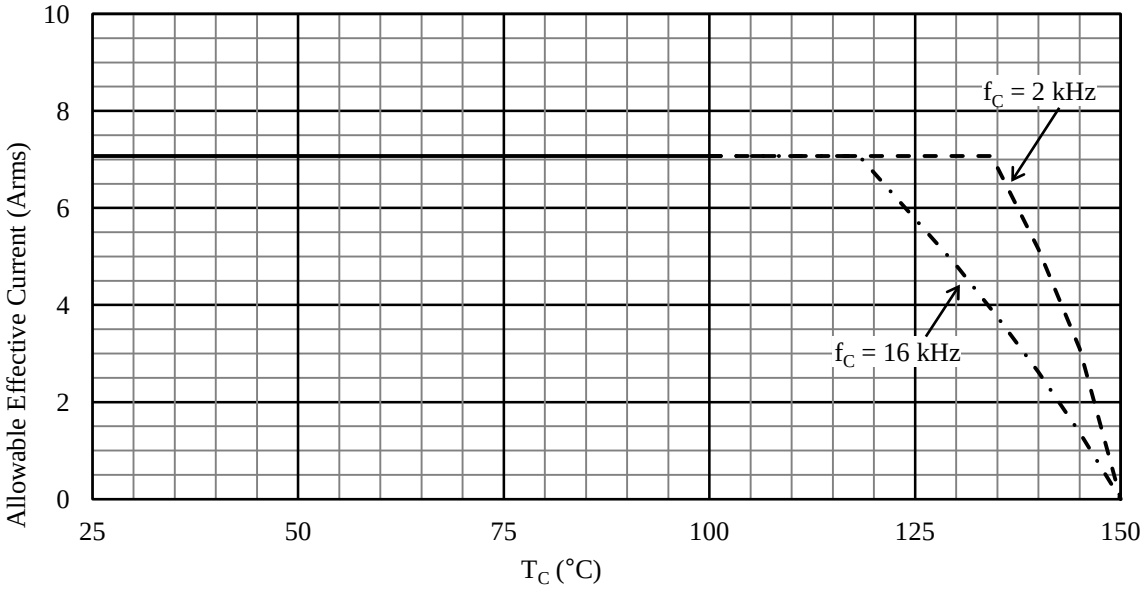


Figure 15-36. SCM3610C11 Allowable Effective Current Curves

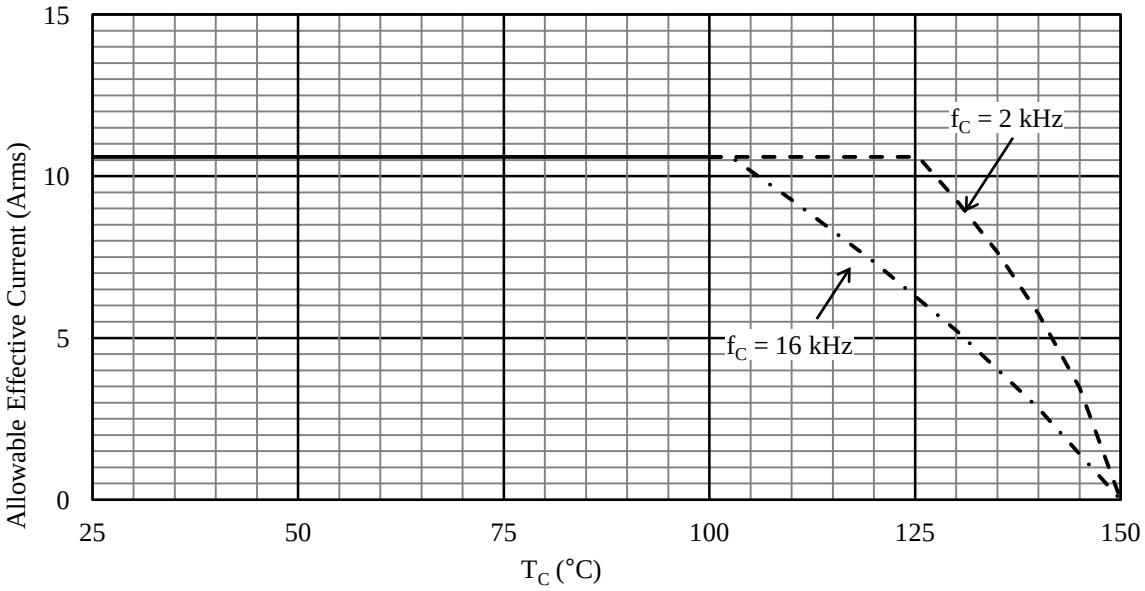


Figure 15-37. Allowable Effective Current Curves

15.5. Short Circuit SOAs (Safe Operating Areas)

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq V_{CC} \leq 16.5$ V, $T_j = 125$ °C, pulse.

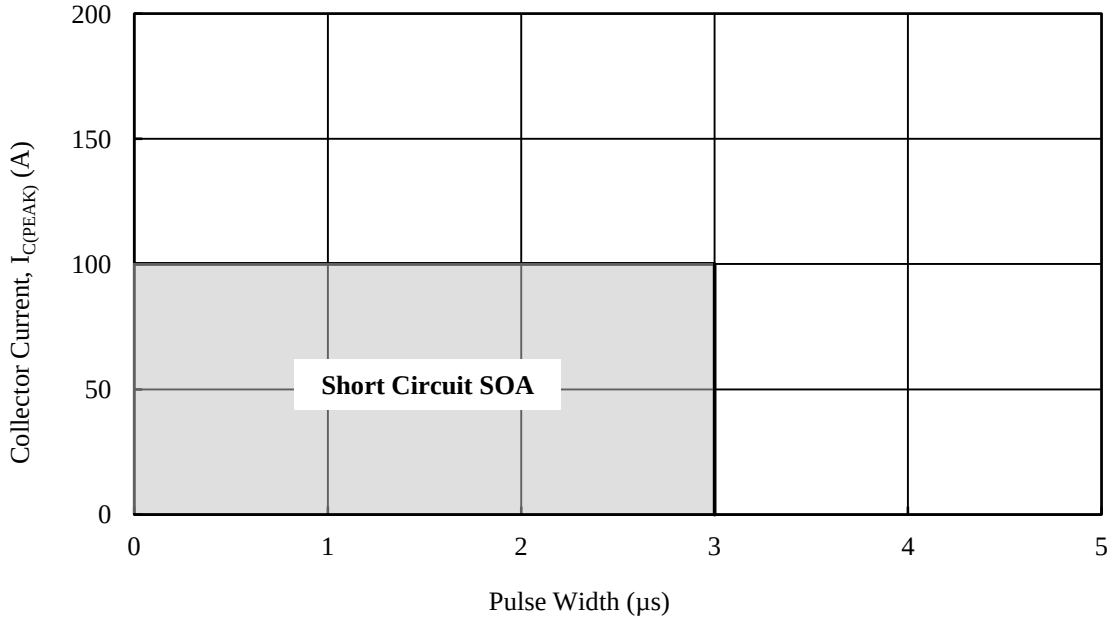


Figure 15-38. SCM3610C11

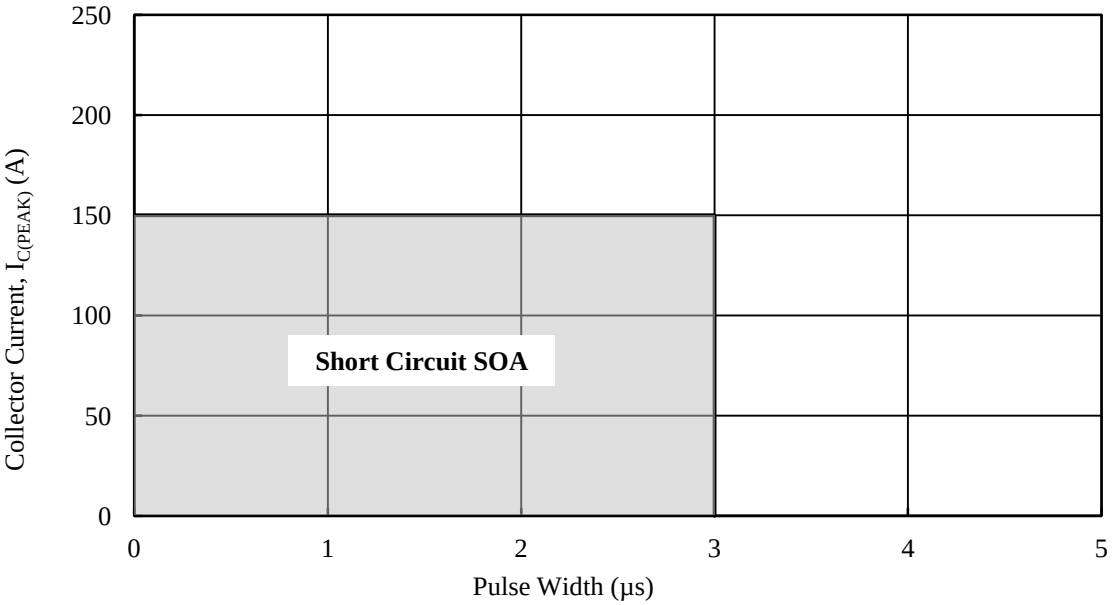


Figure 15-39. SCM3615C11

16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SCM3000C series device. For reference land pattern and terminal hole sizes, see Section 10.2.

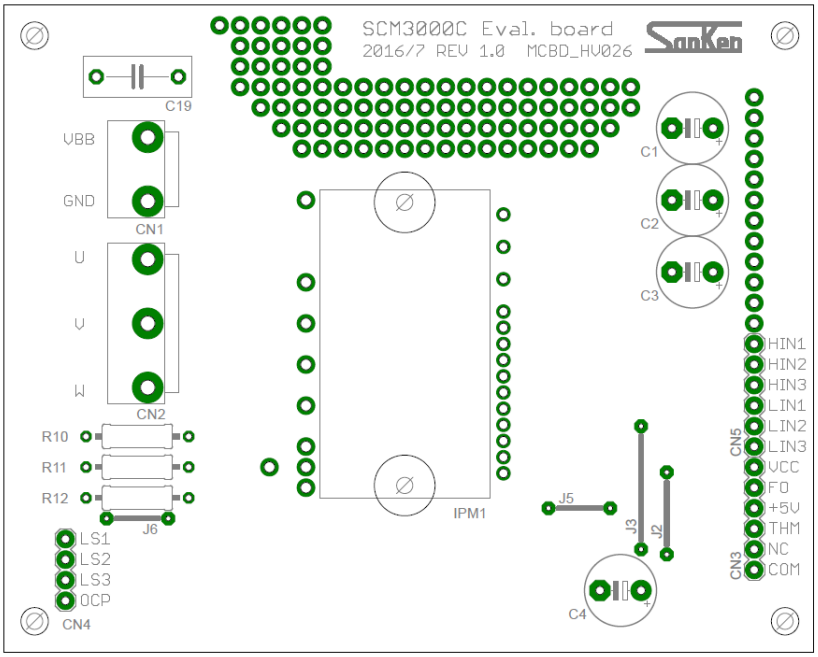


Figure 16-1. Top View

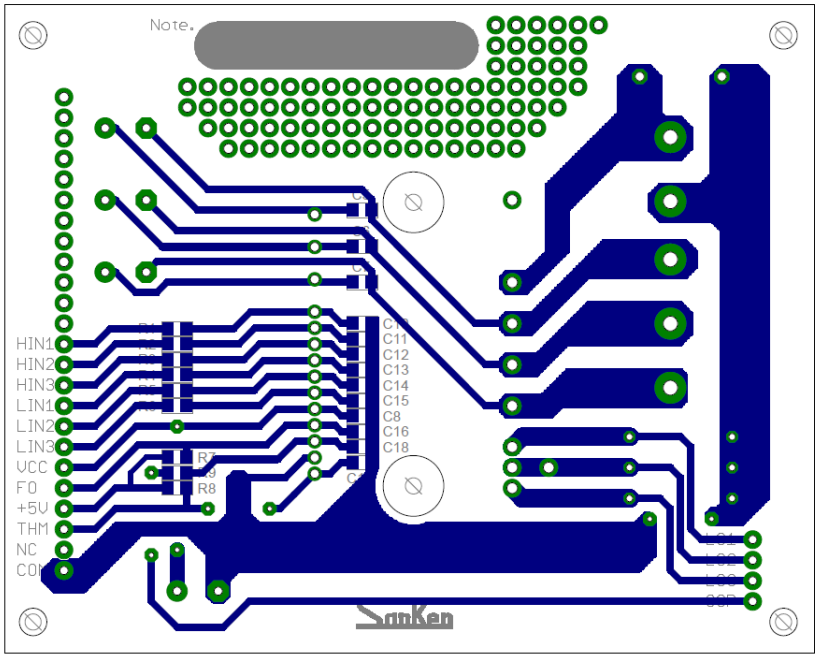


Figure 16-2. Bottom View

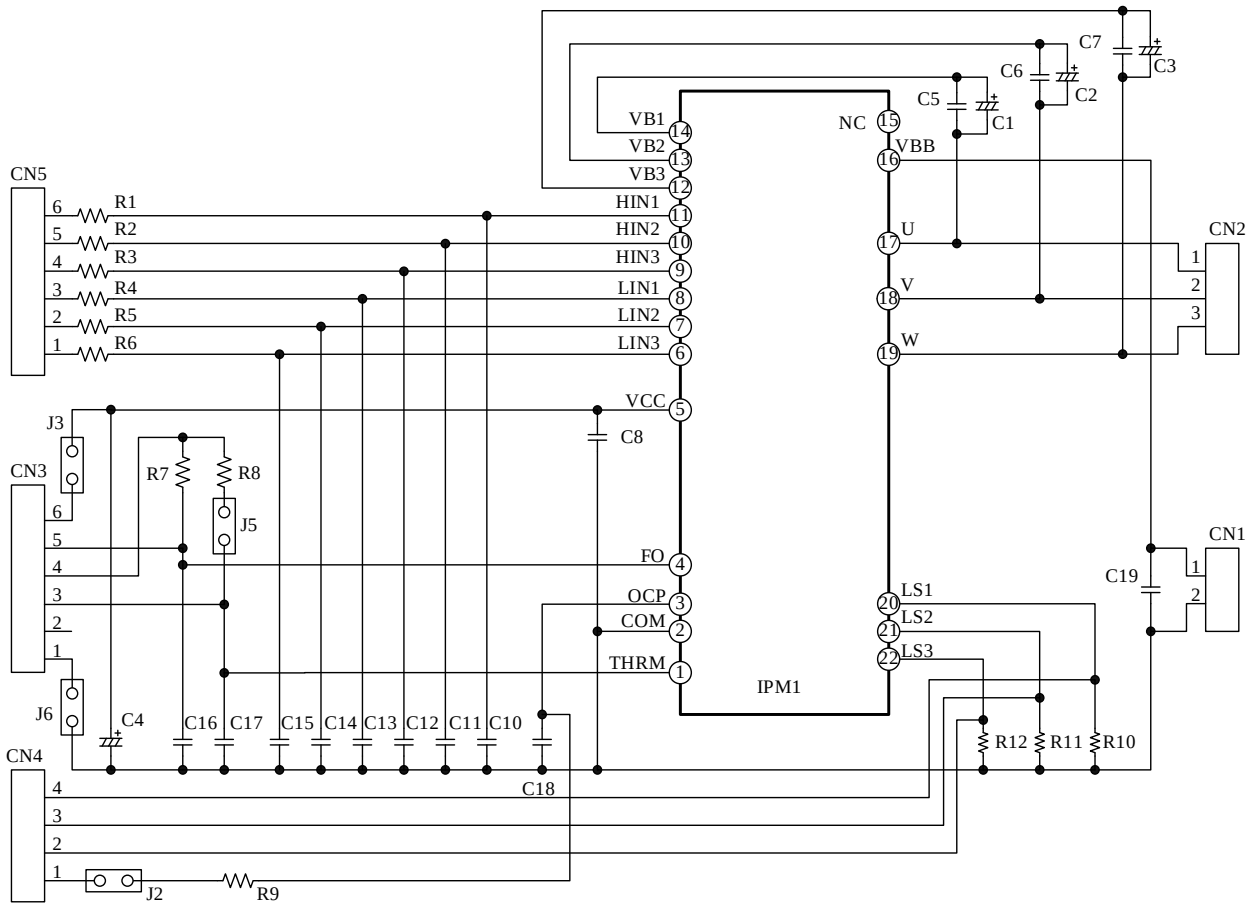


Figure16-3. Circuit Diagram of PCB Pattern Layout Example

17. Typical Motor Driver Application

This section contains information on the typical motor driver application using 3 shunt resistors, including a circuit diagram, specifications, and the bill of the materials used. When implementing the Overcurrent Protection into the circuit diagram in Figure16-3, be sure to follow the guidelines below:

- 3-shunt-resistor Case:
  Use an external comparator (or such component) to detect the outputs from Pins 2 to 4 of CN4, and input them into Pin 1 of CN4.
- 1-shunt-resistor Case:
  Short the IC sides of R10 to R12 (i.e., the LS1, LS2, and LS3 pins), and input any one of Pins 2 to 4 of CN4 into Pin 1 of CN4.

● Motor Driver Specifications

IC	SCM3610C11
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	1.35 kW

● Circuit Diagram

See Figure16-3.

● Bill of Materials (3-shunt-resistor Case)

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	47 µF, 25 V	R1	General	100 Ω, 1/8 W, 2012
C2	Electrolytic	47 µF, 25 V	R2	General	100 Ω, 1/8 W, 2012
C3	Electrolytic	47 µF, 25 V	R3	General	100 Ω, 1/8 W, 2012
C4	Electrolytic	100 µF, 25 V	R4	General	100 Ω, 1/8 W, 2012
C5	Ceramic	0.1 µF, 25 V, 2012	R5	General	100 Ω, 1/8 W, 2012
C6	Ceramic	0.1 µF, 25 V, 2012	R6	General	100 Ω, 1/8 W, 2012
C7	Ceramic	0.1 µF, 25 V, 2012	R7	General	4.7 kΩ, 1/8 W
C8	Ceramic	0.1 µF, 25 V, 2012	R8(1)	General	4.7 kΩ, 1/8 W
C10	Ceramic	100 pF, 50 V, 2012	R9	General	100 Ω, 1/8 W
C11	Ceramic	100 pF, 50 V, 2012	R10(1)(2)	Metal plate	27 mΩ, 2 W
C12	Ceramic	100 pF, 50 V, 2012	R11(1)(2)	Metal plate	27 mΩ, 2 W
C13	Ceramic	100 pF, 50 V, 2012	R12(1)(2)	Metal plate	27 mΩ, 2 W
C14	Ceramic	100 pF, 50 V, 2012	CN1	Connector	Equiv. to B2P3-VH
C15	Ceramic	100 pF, 50 V, 2012	CN2	Connector	Equiv. to B3P5-VH
C16	Ceramic	0.01 µF, 50 V, 2012	CN3	Pin header	Equiv. to MA06-1
C17(1)	Ceramic	4.7 nF, 50 V, 2012	CN4	Pin header	Equiv. to MA04-1
C18	Ceramic	4.7 nF, 50 V, 2012	CN5	Pin header	Equiv. to MA06-1
C19	Ceramic	0.1 µF, 630 V	IPM1	IC	SCM3610C11
			J2, J3, J5, J6	Jumper	Shorted

(1) Refers to a part that requires adjustment based on operation performance in an actual application.
(2) In the application using a single shunt resistor, the sum of the resistors R10 to R12 must be ≥27 mΩ.

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